Design of a DC/DC buck converter for ultra-low power applications in 65nm CMOS Process

Master thesis performed in Electronic Devices
by

Naeim Safari

Report number: LiTH-ISY-EX--12/4547--SE
Linköping, March 2012

Design of a DC/DC buck converter for ultra-low power applications in 65nm CMOS Process

Master thesis
Performed in **Electronic Devices**
Dept. of Electrical Engineering
at **Linköping Institute of Technology**

by

Naeim Safari

LiTH-ISY-EX--12/4547--SE

Supervisor: **Behzad Mesgarzadeh**
Linköping University
Examiner: **Professor Atila Alvandpour**
Linköping University

Linköping, March 2012

Presentation Date

8th March 2012

Publishing Date (Electronic version)

Department and Division

Department of Electrical Engineering
Electronic Devices

Linköpings universitet

Language

✓ English
Other (specify below)

Number of Pages

Type of Publication

Licentiate thesis
✓ Degree thesis
Thesis C-level
Thesis D-level
Report
Other (specify below)

ISBN (Licentiate thesis)

ISRN: LiTH-ISY-EX--12/4547--SE

Title of series (Licentiate thesis)

Series number/ISSN (Licentiate thesis)

URL, Electronic Version
http://www.ep.liu.se

Publication Title

Design of a DC/DC buck converter for ultra-low power applications in 65nm CMOS Process

Author(s)
Naeim Safari

Abstract

Switching mode DC/DC converters are critical building blocks in portable devices and hence their power efficiency, accuracy and cost are a major issue. The primary focus of this thesis is to address these critical issues.

This thesis focuses on the different methods of feedback control loop which are employed in the switching mode DC/DC converters such as voltage mode control and current mode control. It also discusses about the structure of buck converter and tries to find an efficient solution for stepping-down the DC voltage level in ultra-low power applications. Based on this analysis, a 20 MHz voltage mode DC/DC buck converter with an on-chip compensated error amplifier in 65 nm CMOS process is designed and implemented.

The power efficiency has been improved by sizing the power switches to have a low parasitic output and gate capacitances to reduce the capacitive and gate-drive losses. Also the error amplifier biasing current is chosen a small value (12.5 µA) to reduce the power dissipations in the control loop of the system. The maximum 84% power efficiency is achieved at 1.1 V to 500 mV conversion, above 81% efficiency can be achieved at load current from 0.5 mA to 1.26 mA. Due to wide bandwidth error amplifier and proper compensation network the fast transient response with settling time around 45 µs is achieved.

Keywords
DC/DC Converter, Buck, SMPS, Compensation Network, VMC, CMC, ESR, Pulse Width Modulation

Abstract

Switching mode DC/DC converters are critical building blocks in portable devices and hence their power efficiency, accuracy and cost are a major issue. The primary focus of this thesis is to address these critical issues.

This thesis focuses on the different methods of feedback control loop which are employed in the switching mode DC/DC converters such as voltage mode control and current mode control. It also discusses about the structure of buck converter and tries to find an efficient solution for stepping-down the DC voltage level in ultra-low power applications. Based on this analysis, a 20 MHz voltage mode DC/DC buck converter with an on-chip compensated error amplifier in 65 nm CMOS process is designed and implemented.

The power efficiency has been improved by sizing the power switches to have a low parasitic output and gate capacitances to reduce the capacitive and gate-drive losses. Also the error amplifier biasing current is chosen a small value (12.5 µA) to reduce the power dissipations in the control loop of the system. The maximum 84% power efficiency is achieved at 1.1 V to 500 mV conversion, above 81% efficiency can be achieved at load current from 0.5 mA to 1.26 mA. Due to wide bandwidth error amplifier and proper compensation network the fast transient response with settling time around 45 µs is achieved.

Keywords: DC/DC Converter, Buck, SMPS, Compensation Network, VMC, CMC, ESR, Pulse Width Modulation

Acknowledgment

Firstly, I would like to thank Professor Atila Alvandpour for his valuable discussions and support. He has been a source of inspiration for me, his points and thoughtful guidance gave always me a new vision in the field of research.

It is also my pleasure to thank all PhD students in Electronic Devices for their kind help.

I would like to thank all the friends especially to my close friends: Rabia, Afshin, Sepehr, Golnaz, Farid, Kamran, Mahboobeh, Sima, Raheleh and Sahar for the happy moments we shared during my master studies in Linköping.

I am deeply grateful for unconditional love and support by my parents who always encouraged me to pursue my education.

Abbreviations

SMPS	Switching-Mode Power Supply
EMI	Electromagnetic Interference
VMC	Voltage Mode Control
CMC	Current Mode Control
PWM	Pulse Width Modulation
PFM	Pulse Frequency Modulation
HSS	High Side Switch
LSS	Low Side Switch
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
PSM	Power Save Mode
ESR	Equivalent Series Resistance
DCR	DC Resistance
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
DBW	Desired Bandwidth

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Background

DC/DC converters/regulators form the Backbone of different portable electronic devices like cellular phones, laptops, MP3 players which are using batteries as their power supply. Portable devices usually comprise of several sub-circuits that should be supplied with different voltage levels, which are not the same as battery's voltage level which is the main supply voltage.

Employing DC/DC converters can be offered as a method to generate multiple voltage levels from a single DC supply voltage to feed the different sub-circuits in the device. This method of generating multiple voltage levels from a single battery source can reduce the device area substantially [26]. On the other hand DC voltage provided by battery or rectifier contains high voltage ripples and it is not constant enough, thus it is not applicable for most devices. DC/DC regulators are employed to attenuate the ripples regardless of change in the load current or input voltage [1].

Figure 1.1 depicts the block diagram of a general DC/DC regulator which contains two main blocks; power processor and feedback control part. The feedback control part senses the output voltage and adjusts the power transfer by generating corrective control signals to keep the output voltage constant.

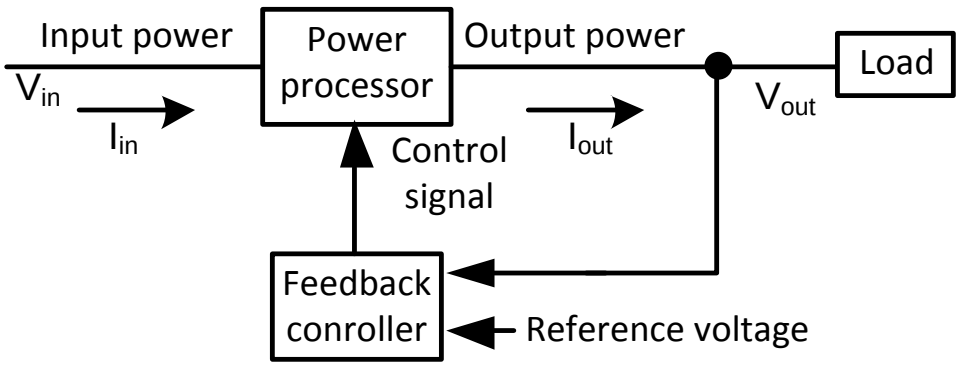

Figure 1.1 Block diagram of DC/DC regulator [2]

1.2 Objective

In this thesis different methods for regulating DC voltage are studied and a DC/DC buck converter for ultra-low power applications is implemented in 65 nm CMOS technology with switching frequency f_{sw}=20 MHz, input voltage 1.1 V and output voltage 500 mV. The main goal of this project is to first study about the switching mode power supplies (SMPS) and different controlling methods which are used nowadays in the circuit of SMPS, then implement a buck converter and try to enhance the buck converter's power efficiency. Scaling down the passive components like inductor's size without sacrificing the system's overall performance is another purpose of this thesis.

1.3 Thesis outline

The rest chapters of the thesis are organized as follows:

Chapter 2 discusses on the different DC to DC conversion methods and illustrates their architectures.

Chapter 3 explains the structure of DC/DC buck converter and describes the different parts of the converter's circuit.

Chapter 4 discusses about the practical issues involved in designing a buck converter such as power efficiency, duty cycle and stability criteria. It also describes different control methods like Voltage Mode Control, Current Mode Control, Pulse Width Modulation and Pulse Frequency Modulation techniques which are used for regulating output voltage.

Chapter 5 shows the implementation and performance evaluation of a buck converter.

Finally chapter 6 presents conclusions on this thesis work and discusses about future work.

Chapter 2

DC/DC Conversion methods

SMPS and linear regulators are two main methods which are employed to convert an unregulated DC voltage to a regulated DC level, regardless of changes in load current and input voltage. In this chapter we will discuss different methods of DC/DC conversion and explain their advantages and drawbacks.

2.1 Linear regulator

Linear regulator is a type of power supply which instead of using switches, employs voltage divider network for adjusting output voltage. Figure 2.1 shows the block diagram of a linear regulator which includes two main parts:

1) The regulating part that is a simple variable resistance (usually transistor which operates in linear region) in series with the output load to adjust output voltage [4].

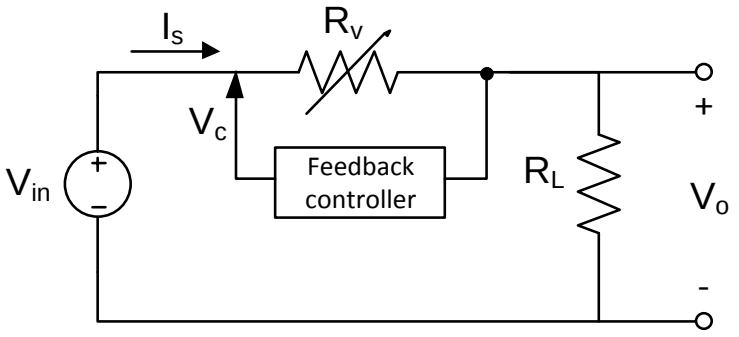

Figure 2.1 Linear regulator diagram [25]

2) As shown in Figure 2.2, the control part is a VCCS (voltage controlled current source) which senses the output voltage V_o and regulates the current source I_s to keep the output voltage equal to the set reference value V_{ref} [5].

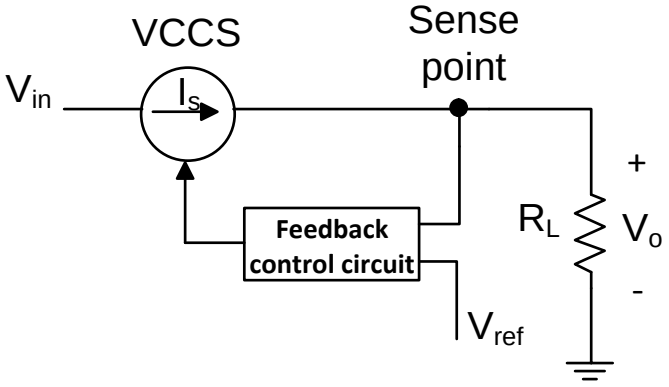

Figure 2.2 Typical linear regulator [5]

Unlike the switching-mode power supply, the linear regulator operates continuously, thus its efficiency is less than switching regulator and it produces much more heat comparison to SMPS. For example let's assume that the input voltage and current of a linear regulator are respectively 5v and 5A and we need 2v at the output. This demands the linear regulator to dissipate 3v × 5A=15w power across the variable resistance as heat to regulate output voltage and hence a large volume heat-sink would be required to reduce the circuit's temperature. Whenever the difference between the input and output voltage is larger, the more heat is produced, which must be dissipated with bulky and expensive heat-sinks.

2.2 SMPS (Switching-Mode Power Supply)

Switching-mode power supply which is also called as switching-mode DC to DC converter is a type of power supply which uses switches (usually in the form of transistor) and low loss components such as inductors, capacitors and transformers for regulating output voltage [3]. The circuit of SMPS consists of two main parts: power stage and control part. Nowadays most of the work is done on control part for better regulation of output voltage, whereas the power part has not undergone many changes.

Usually MOSFET is used as a power switch in SMPS for stabilizing output voltage. The switches are not conducted continuously and they operate under specific frequency, therefore they are useful for conservation of battery life and reduction of the power loss in the circuit.

Depending on the structure of SMPS, it can be used for stepping down or up of DC input voltage. The switching-mode power supply usually consists of a low pass filter at the output stage for suppressing the ripples due to switching otherwise huge ripples will appear at the both output voltage and current. Figure 2.3 illustrates the block diagram of a typical switching-mode power supply.

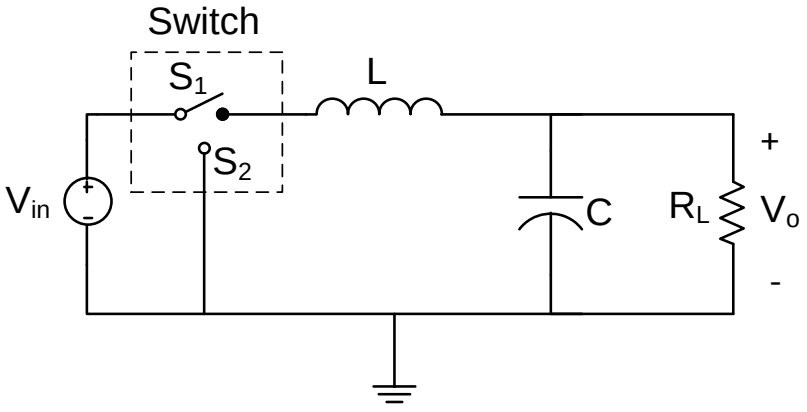

Figure 2.3 Switching-mode power supply

2.3 Switching regulator vs. linear regulator

The following reasons vividly demonstrate why the switching regulator is the only reasonable choice compared with a linear regulator:

- **Higher Power efficiency**

Linear regulator uses voltage drop across series passive element to regulate output voltage. Therefore excess power is dissipated in the form of heat which requires a large volume heat-sink to reduce the circuit's temperature; whereas SMPS uses switching technique to suppress the extra power. Since the switches are not continuously conducted (depends on the switching duty cycle), it losses much less power comparison to linear regulator.

The Power efficiency in both SMPS and linear regulator is expressed in equation 2.1:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out}.I_{out}}{V_{in}.I_{in}} \ \% \qquad (Eq.\ 2.1)$$

Where P_{out} is the output power, P_{in} is the input power, V_{out} is the output voltage, I_{out} is the load current, V_{in} is the input supply voltage and I_{in} is the input current. Since in the linear regulators input current and output current have the same value ($I_{out} = I_{in}$) therefore "Eq. 2.1" can be simplified to "Eq.2.2" for a linear regulator

$$\Longrightarrow \eta = \frac{V_{out}}{V_{in}} \ \% \qquad (Eq.\ 2.2)$$

Based on equation 2.2, we can easily find that the efficiency of a linear regulator is directly related to the power drop across its variable resistance. Therefore whenever the difference between input and output voltage is high the efficiency of linear regulators can be significantly reduced which means reduction in battery life for any application [30].

- **Versatility**

The energy stored by the output inductor of a SMPS can be transformed to output voltage, which can be greater than input voltage (stepped-up), or lower than input voltage (stepped-down) or even converted to a negative voltage; however the linear regulator is only able to step-down the dc voltage level.

SMPS drawbacks

Of course, SMPS is not without its drawbacks; although the size and weight of the switching-mode power supply is smaller than linear regulator but it requires a more complicated feedback control loop compared to linear regulator for energy management. This causes increase in overall cost of the power supply and makes it more expensive than linear one.

The main concern in the switching-mode power supply is Electromagnetic Interference (EMI) noise caused by the fast transitions of current and voltage due to high frequency

switching. Rapid voltage changes at the inductor node leads to radiated electric fields, while fast-changing inductor current produces magnetic fields [30]. Output voltage ripples at the switching frequency is another issue which is needed to be filtered out with an extra LC filter.

Chapter 3

DC/DC Buck converter

3.1 Introduction

Buck converter is a type of switching-mode power supply which is used for stepping-down DC voltage level. Switch controller block and power block are two main parts of buck converter's circuit. "It can operate in Continuous Conduction Mode (CCM) or in Discontinuous Conduction Mode (DCM), depending on the waveform of the inductor current [1]". Voltage Mode Control (VMC) and Current Mode Control (CMC) are two main methods to control switching. Both of these two methods can be applied with either PWM (Pulse width modulation) or PFM (pulse frequency modulation) techniques. The PFM is more efficient when the load current is too low.

Figure 3.1 depicts the DC/DC buck converter circuit. As can be seen it is included a switch controller block, high side power switch S_1, low side power switch S_2 , inductor L, output capacitor C, and load resistance R_L.

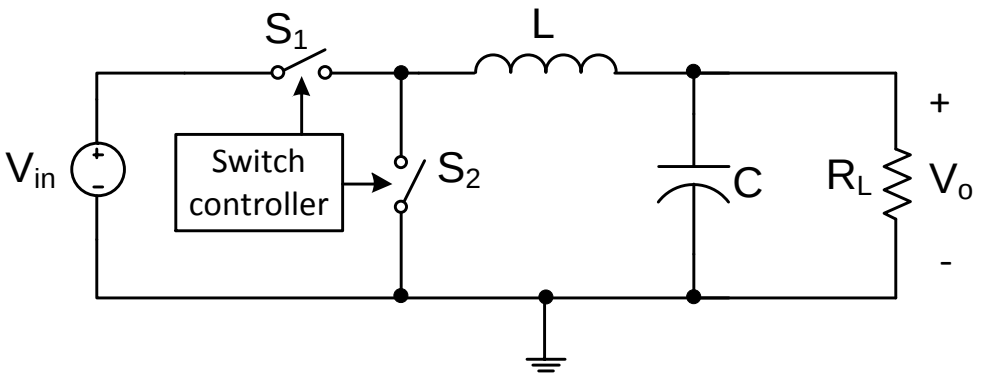

Figure 3.1 Buck converter

Usually P-channel MOSFET (PMOS) is preferred to be used as a high side switch (HSS) instead of NMOS, because if the NMOS is employed as a high side switch since both the gate and the source are connected to the voltage supply then it would be hard to drive it [1].

The diode (which is used in conventional buck converters) is usually replaced by an n-channel MOSFET (NMOS) as a low side switch to improve power efficiency of converter. Since voltage drop in conducted MOSFET is very low comparison to conducted diode (even from Schottky diode which has low forward voltage drop), the total power loss in DC/DC converter will be significantly reduced by this replacement. Figure 3.2 illustrates the schematic model of a generic buck converter.

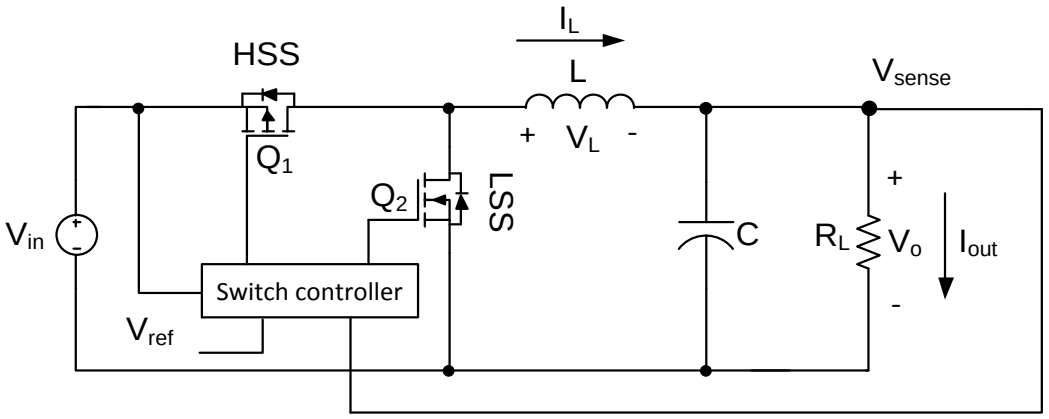

Figure 3.2 Buck converter schematic

Procedure:

When high side switch Q_1 is on, a path will be provided for the DC input voltage to charge the inductor and supplies the load current. Charging will continue till the output voltage reaches to reference voltage V_{ref}, then the control part turns off the high side switch to keep the output voltage close to V_{ref}. Therefore there is no path to charge inductor, and then inductor changes its voltage polarity and the current flows in the same direction through the low side switch Q_2 which is turned on by switch controller part. Discharging will continue until the output voltage reaches below of the reference voltage, then control part again turns on the high side MOSFET to compensate the output voltage drop and this cycle continues until complete regulation of output voltage [10].

This process is accomplished by sensing the output voltage of the circuit by means of a negative feedback loop which adjusts the duty cycle (Eq.3.1) to control on and off state of the MOSFET switches under specified frequency f_{sw} [1].

$$D = \frac{t_{on}}{T} = \frac{t_{on}}{t_{on} + t_{off}} = f_{sw}.t_{on} \qquad (Eq.3.1)$$

Where t_{on} is the time interval that power MOSFET Q_1 conducts (on-state), t_{off} is the time interval that Q_1 is open (off-state), T is the period and f_{sw} is the switching frequency.

3.2 Description of different components of buck converter

3.2.1 PWM switch controller

The PWM generator is the major part in DC/DC converters. It controls the switches' ON and OFF state to regulate the output voltage, in other words by changing the duty cycle tries to keep output voltage equal to set reference voltage. For example in a buck converter if the reference voltage V_{ref} is set to low voltage the PWM generator reduces the duty cycle by holding on the HSS for a short time of every cycle. While the output reference voltage V_{ref} is high, the PWM generator increases the duty cycle by holding on the HSS for the most of

cycle to rectify the output voltage. Figure 3.3 shows the schematic model of a PWM buck converter.

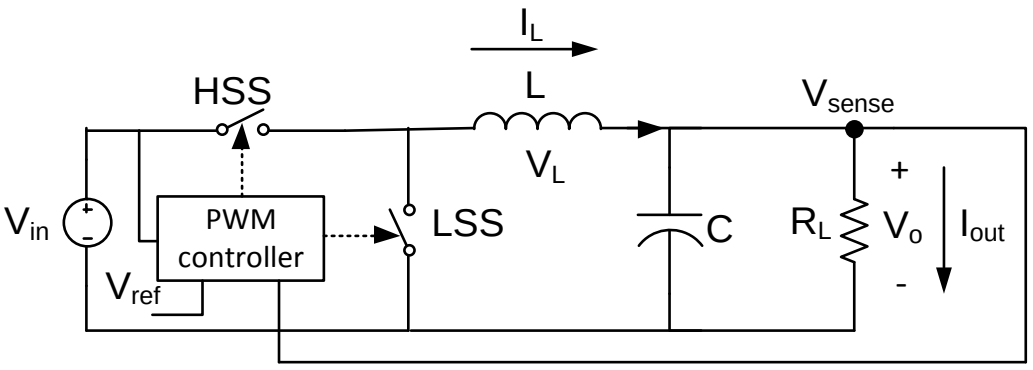

Figure 3.3 PWM Buck converter schematic

Architecture

As shown in figure 3.4, PWM controller contains two main parts; voltage error-amplifier and voltage comparator. The error-amplifier compares the feedback voltage V_F(applied to inverting input) to reference voltage V_{ref} (applied to non-inverting input) then their difference which is called voltage error signal V_E after amplification is applied to non-inverting input of voltage comparator. Comparator compares this error voltage to sawtooth ramp V_{saw} that is generated by ramp generator, if voltage V_E is higher than V_{saw} output voltage of comparator goes high but when V_E is lower than V_{saw} the output of comparator goes low to adjust the switching duty cycle.

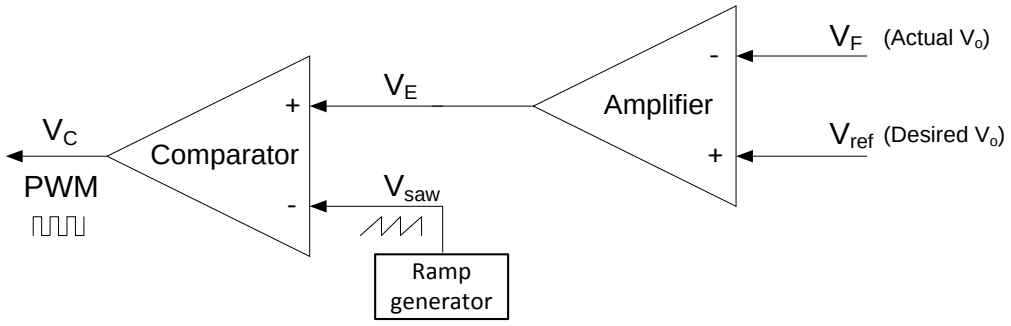

Figure 3.4 PWM generator configuration [1]

Error voltage V_E is inversely proportional to voltage reference V_{ref}, for example when V_{ref} is low, error voltage V_E is increased by error amplifier to adjust the switching duty cycle. As can be seen in figure 3.5 when the error voltage is high the pulse width of PWM wave at the output of voltage comparator (V_C) is increased to keep off High side switch (PMOS) for the most time of the each cycle in order to reduce duty cycle to regulate output voltage. Vice versa as shown in figure 3.6 when V_{ref} is high error amplifier reduces V_E to keep on the HSS for a most time of each period in order to adjust output voltage [14].

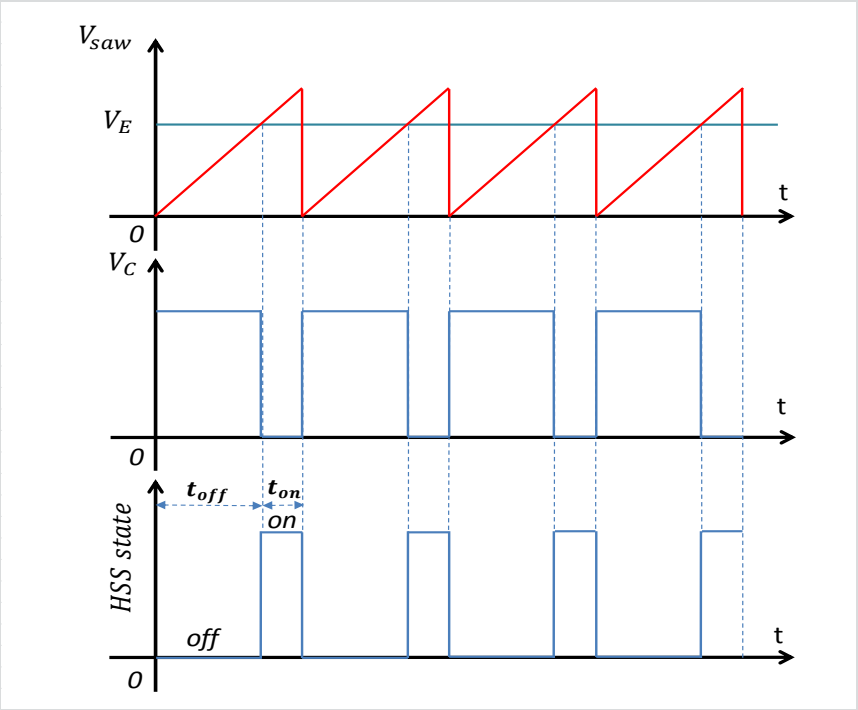

Figure 3.5 Duty cycle waveform when V_{ref} is low

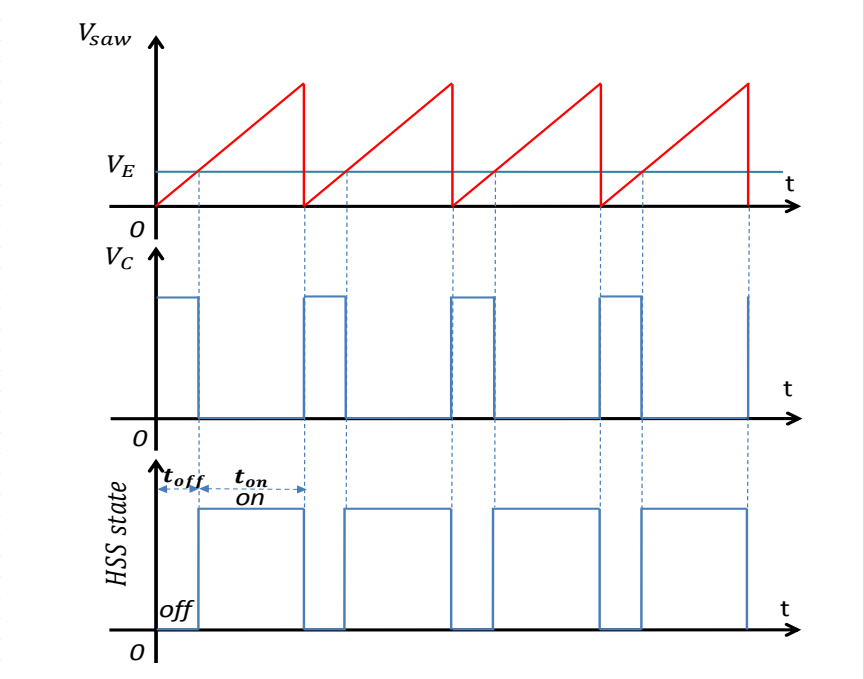

Figure 3.6 Duty cycle waveform when V_{ref} is high

3.2.2 Power stage

Power stage consists of several parts such as low and high side switches, gate-driver, output LC filter and the load. PMOS is used for high side switch and NMOS for Low side switch.

The power PMOS and NMOS are large enough to have lower drain-source on resistance (lower $R_{DS\ on}$) to reduce switching power loss during conduction state.

Driver is one of the major parts in DC/DC converter, it acts like current buffer and makes the PWM waveform (generated by voltage comparator) smoother to turn on and off the power PMOS and NMOS switches quickly to avoid energy dissipation during transition. Gate-driver can be included tapered chain of the inverters with a proper transistor sizing with respect to power switches size.

The major issue in the designing driver is the power dissipation during transition signal, since the signal toggles between the inverters power loss is inevitable in the driver. Power dissipation in the power switches and gate-driver is considerable compared to other part of converter. Therefore designers always try to enhance the converter power efficiency by sizing of power MOSFETs and modification of the driver stages with some techniques in order to reduce the power consumption [15].

3.2.3 Inductor

Output inductor in the Buck converter in addition to being a part of the low-pass filter for removing switching ripples from the output voltage, has two essential tasks:

1) "Limiting the current slew rate through power switches" which yields limiting in the peak current. This action reduces power loss in the circuit [6].

Whatever the inductor size is larger the peak inductor current and its ripple will be reduced, which yields enhancement in the converter's efficiency. But always there is a trade-off between the size of inductor and efficiency of DC/DC converter. On the other hand we have limitation for minimizing inductor size otherwise converter cannot work properly, for example the inductor current ripple will be increased which causes increase in power losses in the inductor and the power MOSFETs, therefore we can consider a boundary to select proper inductor size for having a higher efficiency and lower occupied area in the circuit.

2) The main advantage of employing inductor in switching mode power supply is "Storing energy" [6].

Due to 90 degree phase difference between the current and voltage through the inductor, energy can be saved during charging interval and then can be recovered in the discharging interval. This energy can be calculated in Joules by

$$E = \frac{1}{2}.L.I^2 \qquad (Eq.3.2)$$

Where 'I' is the current through inductor and 'L' is the inductance value [6].

3.2.4 Capacitor

Capacitor is employed at the output stage of buck converter to minimize the voltage ripple and overshoot appear across the load. The capacitor should be large enough to prevent

noticeable change in its voltage during discharging interval, so there is a limitation for minimizing the size of capacitor otherwise huge voltage ripple and overshoot will appear at the output stage. “Large overshoots are caused by insufficient output capacitance, and large voltage ripple is caused by insufficient capacitance as well as a high equivalent series resistance (ESR) in the output capacitor [33].”

The maximum allowed output voltage overshoot and ripple are usually part of buck converter’s design specifications. Therefore, to meet the ripple specification for a buck converter circuit, the output capacitor should be selected with a sufficient capacitance and low ESR. On the other hand choosing an output capacitor with very low ESR may cause instability in the buck converter’s system. In chapter 4 it will be discussed in more details that how ESR value can affect the stability of the converter’s system.

Chapter 4

Practical issues of buck converter

4.1 Power loss and efficiency

The efficiency of DC/DC converter is always main concern which is considered by power designers. They try to use different techniques to reduce power loss in different components like the power switches to increase power efficiency of the converter. The majority of the power dissipation in the DC/DC converter occurs through power switches which is included conduction loss P_{con} and switching loss P_{sw}. The total power loss in power switches is determined in equation 4.1 [11].

$$P_{loss} = P_{con} + P_{sw} \qquad (Eq.\,4.1)$$

The power loss due to High side switch (PMOS) in DC/DC buck converter can be described from the following equation;

$$P_{loss_{HS}} = \underbrace{R_{DS(on)}.{I_{out}}^2.D}_{\boldsymbol{P_{con}}} + \underbrace{\frac{(V_{in}.I_{out})}{2}\left(t_r + t_f\right).f_{sw} + C_{oss}.f_{sw}.{V_{in}}^2}_{\boldsymbol{P_{sw}}} \qquad (Eq.\,4.2)$$

Where $R_{DS(on)}$ is the MOSFET drain-source on-state resistance, I_{out} is the output current, D is the power switch's duty cycle, V_{in} is the input voltage, t_r is the MOSFET rise time, t_f is the MOSFET fall time, f_{sw} is the switching frequency and C_{oss} is the MOSFET output capacitance ($C_{DS} + C_{DG}$) [11], [12].

As shown in equation 4.2, the first expression is correlated to conduction loss and the second part represents the switching loss of the high side MOSFET. As can be seen the conduction loss is directly proportional to the duty cycle and the MOSFET drain-source on-state resistance thus reduction in value of "$R_{DS(on)}$" and "D" have an important role to reduce the total power loss in the high side power switch. On the other hand power switching loss is directly proportional to the switching frequency and therefore by increasing the switching frequency the power dissipation increases.

While the total power loss via the low side switch (NMOS) in the buck converter (during off-state) can be achieved from equation 4.3:

$$P_{loss_{LS}} = R_{DS(on)}.{I_{out}}^2.(1 - D) \qquad (Eq.\,4.3)$$

The total power loss of the Low side MOSFET is directly proportional to the MOSFET drain-source on-state resistance but inversely proportional to the switching duty cycle. The switching power loss is negligible because the Low side NMOS switches with just its body diode (forward conduction) which does not dissipate significant power and so it can be safely ignored [11].

4.2 Duty Cycle calculation for buck converter:

First we assume that both LSS and HSS are ideal and other elements are lossless;

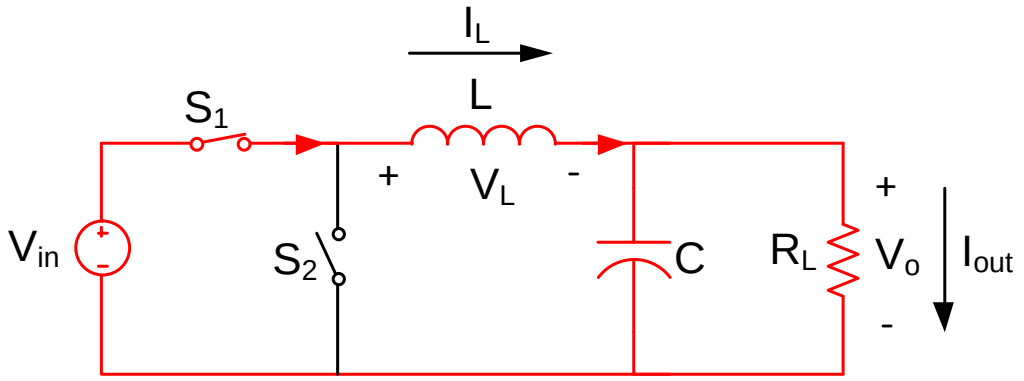

Figure 4.1 Buck converter configuration (on-state) [13]

As shown in figure 4.1, when the high side MOSFET conducts (during on-state) the path is provided to supply inductor and load. On the other hand, since the low side MOSFET is switched OFF (cut-off state) by PWM controller part thus there is no current flow through it and in this condition inductor current increases linearly and voltage "$V_{in} - V_O$" appears across the inductor [13]. Energy stored in inductor can be described from equation 4.4:

$$E = {}^{1}/_{2}\, L \times {I_L}^2 \qquad (Eq.\ 4.4)$$

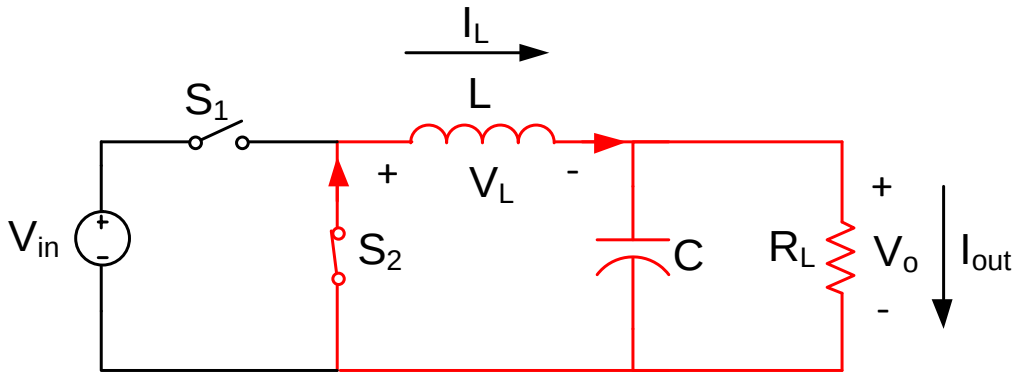

Figure 4.2 Buck converter configuration (off-state) [13]

As illustrated in Figure 4.2, when the high side switch is turned off (during off-state) and low side one is turned on a path will be provided to discharge energy which is stored in inductor, so the inductor current decreases and voltage "$-V_O$" appears across the inductor [13].

Figure 4.3 shows the inductor voltage and current waveforms in both on and off states.

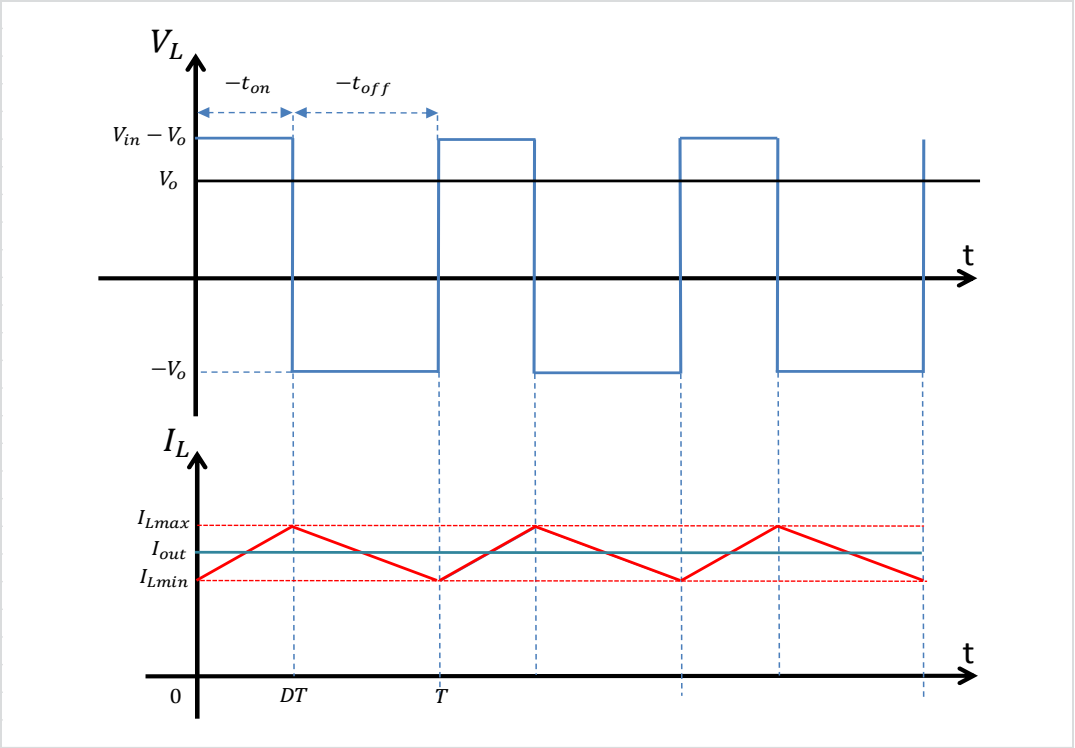

Figure 4.3 Inductor voltage and current waveforms in "on & off" states [13]

Therefore according to faraday's law (Eq.5.1) we can calculate the amount of increase in the inductor current during on-state ($\Delta I_{L_{ON}}$) and decrease during off-state ($\Delta I_{L_{OFF}}$) from equations 4.5 and 4.6 [13]:

$$\Delta I_{L_{ON}} = \int_0^{t_{ON}} \frac{V_L}{L} dt = \frac{(V_{in} - V_o)}{L} t_{ON} \qquad (Eq. 4.5)$$

$$\Delta I_{L_{OFF}} = \int_0^{t_{OFF}} \frac{V_L}{L} dt = \frac{(-V_o)}{L} t_{OFF} \qquad (Eq. 4.6)$$

If we assume that converter operates in steady-state, so inductor current is the same at start ($I_{L_{t_0}}$) and at the end (I_{L_T}) of period:

$$I_{L_{t_0}} = I_{L_T} \qquad (Eq. 4.7)$$

It means that energy stored in inductor at the end of cycle is equal to energy which is stored at the start of cycle, so from equation 4.7:

$$\frac{(V_{in} - V_o)}{L} t_{ON} - \frac{V_o}{L} t_{OFF} = 0 \qquad (Eq. 4.8)$$

The on-state and off-state time intervals can be determined from equation 4.9 and equation 4.10 respectively:

$$t_{ON} = D.T \quad \text{(Eq. 4.9)}$$

$$t_{OFF} = (1 - D)T \quad (Eq. 4.10)$$

By inserting these two equations into Equation 4.8 the duty cycle can be easily obtained from equation 4.11 [13]:

$$\Longrightarrow D = \frac{V_o}{V_{in}} \quad (Eq. 4.11)$$

4.3 Compensation and stability criteria

To ensure stability in the control feedback loop of converter the compensation circuit is necessary, because without compensation part always there is a possibility that variation in input leads to instability in the system, which avoids achieving optimum regulation performance. Improving phase margin (by generating zero in the system's transfer function) to make converter unconditionally stable and enhancing the gain at low frequencies (below the cross-over frequency) to attain converter's output voltage very close to reference voltage are the two main purposes of using compensation technique [16].

For assurance the system's control loop stability following cases are considerable;

- In the worst-case the system at least should have phase margin $35° \; to \; 45 \; °$ [4] (preferably $45° \; to \; 60 \; °$) [1].
- Typically gain margin -6 dB to -12 dB is enough to ensure stability in the overall loop.
- The crossover frequency should be less than half of switching frequency, but practically it is chosen less than that, preferably $1/4$ or $1/5$ of switching frequency otherwise there will be huge switching ripples at the output voltage [4].
- Typically the system is stable if the gain transient response crosses the unity gain(0 dB) with slope of -20 dB/dec (not more than -20 dB/dec) [17].
- The error amplifier should have enough attenuation at switching frequency to ovoid amplification of the output voltage ripples [17].
- The compensation gain should not be more than the error amplifier open loop gain since this is the limiting factor of the compensation circuit [18].

An important point that should be taken in account about PM of control loop is that "a lower phase margin gives faster transient response and shorter settling time, but more peaking in the closed-loop transfer function and higher ringing and overshoot in the transient responses [1]". Thus there is a tradesoff in choosing a desired PM by considering settling time and ripples in the output voltage, generally PM $60 \; °$ is chosen [19] to attain faster transient response and lower overshoot and peaks at the output voltage.

Generally three types of compensator error amplifier are employed (depends on different condition) in DC/DC buck converter's control loop; type I, type II and type III. Type I

which is also referred as a single pole compensation is not too much practical due to its limited bandwidth and low phase margin however it has high DC gain at low frequencies, therefore type II or type III are more preferable to enhance the bandwidth and improve the phase margin of system's closed-loop to ensure stability.

Type II has fewer elements compared to type III and it is useful when the output filter capacitor of the converter C has high ESR whereas type III is usually employed when ESR is low (ESR zero frequency f_{ESR} is high) [20]. In other words if the zero generated by capacitor ESR provides enough phase boost at crossover frequency type II will suffice, while if phase boost provided by capacitor ESR in not enough then another zero will be added by means of type III (for compensation the system's closed-loop phase).

4.3.1 Type I compensator

As can be seen in figure 4.4, the first type of compensation is a pure integrator op-Amp. If the output voltage of the system is not equal to reference voltage (less than reference voltage V_{ref}) then R_{bias} will be connected between the inverting input of the error amplifier and ground as a voltage programming resistor to offset and adjust steady-state value of output voltage to make it closer to reference voltage. R_{bias} has no effect on the compensation performance and can be ignored when it is not needed [16].

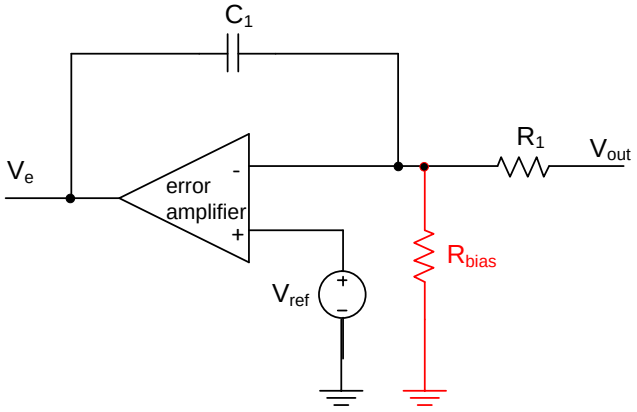

Figure 4.4 Type I compensation network [16]

4.3.1.1 Transfer function of type I compensator

The transfer function of type I compensator has one pole at the origin thus for all frequencies it falls at slope -20 dB/dec and its phase shift is constant '$-90°$'at all frequencies. Figure 4.5 shows the bode plot of Type I compensator.

$$\frac{V_E}{V_{out}} = -\frac{1}{R_1 C_1 s} \qquad (Eq.4.12)$$

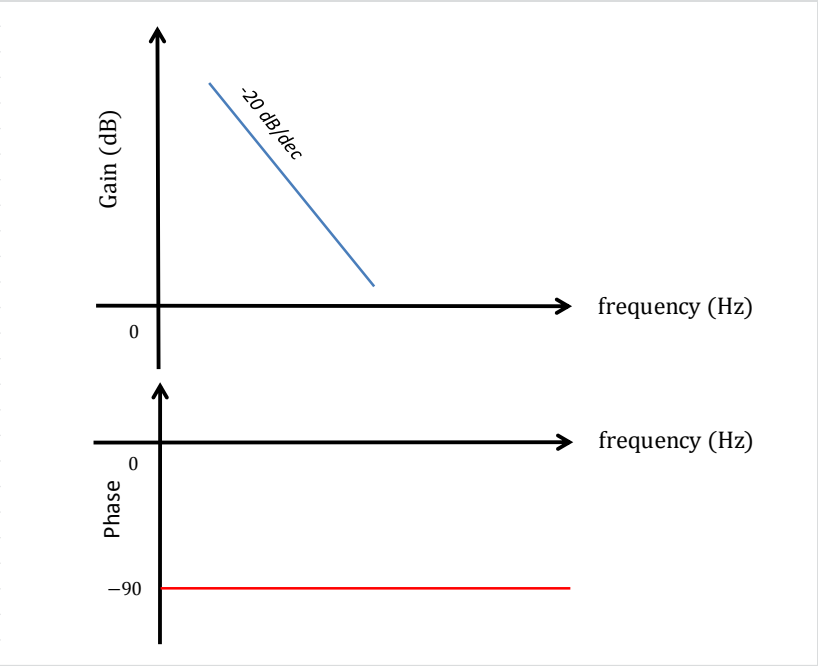

Figure 4.5 Bode plot of Type I compensator

4.3.2 Type II compensator

Type II compensator which is also called second-order integral-lead controller is depicted in figure 4.6;

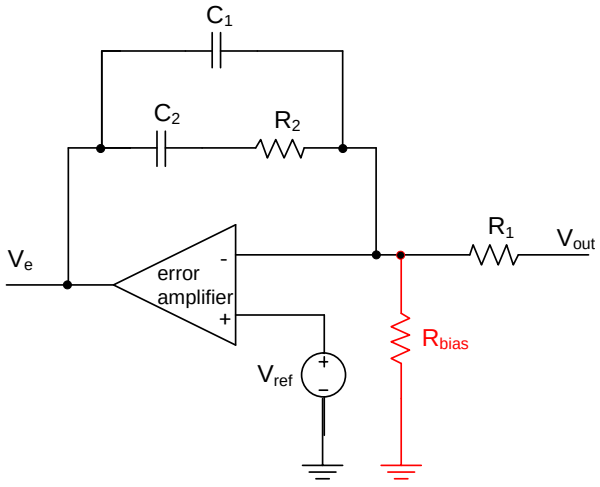

Figure 4.6 Type II compensation network [18]

This type of compensation is employed when phase boost provided by output filter capacitance's ESR is enough. (ESR is relatively high).

4.3.2.1 Transfer function of type II compensator

The transfer function of type II compensator has a pole at the origin which makes integral part and a single pole-zero pair that makes the lead part of the compensator. The resistance R_1 and capacitor C_1 which provides a pole at the origin, form the integral part of compensator circuit. The capacitor C_2 and the resistance R_2 provide a zero. Also the resistance R_2 and the series combination of capacitor C_2 and the capacitor C_1 provide a pole, the capacitor C_1 is usually chosen much smaller than the capacitor C_2 thus the zero frequency f_{zc_2} is much lower than the pole frequency f_{pc_2} [1].

The purpose of using integral part in compensator circuit is to attain higher gain at low frequencies (and at DC) in order to reduce DC error but its drawback is reduction of stability in the system. This is due to the fact that the integral controller leads to phase shift $-90\,°$ (phase lag) in all frequencies so for counteracting or reducing the phase lag between zero and pole frequencies of the system, employing lead compensator is the best option. Overall the duty of the lead compensator is to increase the gain crossover frequency f_c by introducing a zero at the right side of the pole ($f_p > f_z$) to meet the desired phase margin. Increasing the gain crossover frequency leads to achieve a wide bandwidth and fast transient response of the system [1].

If we assume that error-amplifier is ideal the current through the impedance Z_2 and resistance R_1 is equal thus the transfer function of type II compensator can be obtained by a simple calculation;

$$\frac{V_{out}}{R_1} = -\frac{V_E}{Z_2} \qquad (Eq.4.13)$$

The impedance Z_2 can be determined from equation 4.14:

$$Z_2 = \left(R_2 + \frac{1}{C_2 s}\right) || \frac{1}{C_1 s} \qquad (Eq.4.14)$$

By inserting Z_2 into equation 4.13 the transfer function of type II compensation network can be achieved from equation 4.16:

$$\Rightarrow \frac{V_{out}}{R_1} = -\frac{V_E}{\left(R_2 + \frac{1}{C_2 s}\right) || \frac{1}{C_1 s}} \qquad (Eq.4.15)$$

From equation 4.15:

$$\frac{V_E}{V_{out}} = -\frac{1}{R_1 C_1} . \frac{s + \frac{1}{R_2 C_2}}{s.\left(s + \frac{C_1 + C_2}{R_2 C_1 C_2}\right)} \qquad (Eq.4.16)$$

As can be seen in equation 4.16 the transfer function of Type II has a pole at origin and one single zero at frequency:

$$f_{zc_2} = \frac{1}{2\pi R_2 C_2} \qquad (Eq.4.17)$$

And a single pole at frequency:

$$f_{pc_2} = \frac{C_1 + C_2}{2\pi C_1 C_2 R_2} \qquad (Eq.4.18)$$

Figure 4.7 illustrates the bode plot of Type II compensator and shows that it gives a $90°$ phase boost [18]:

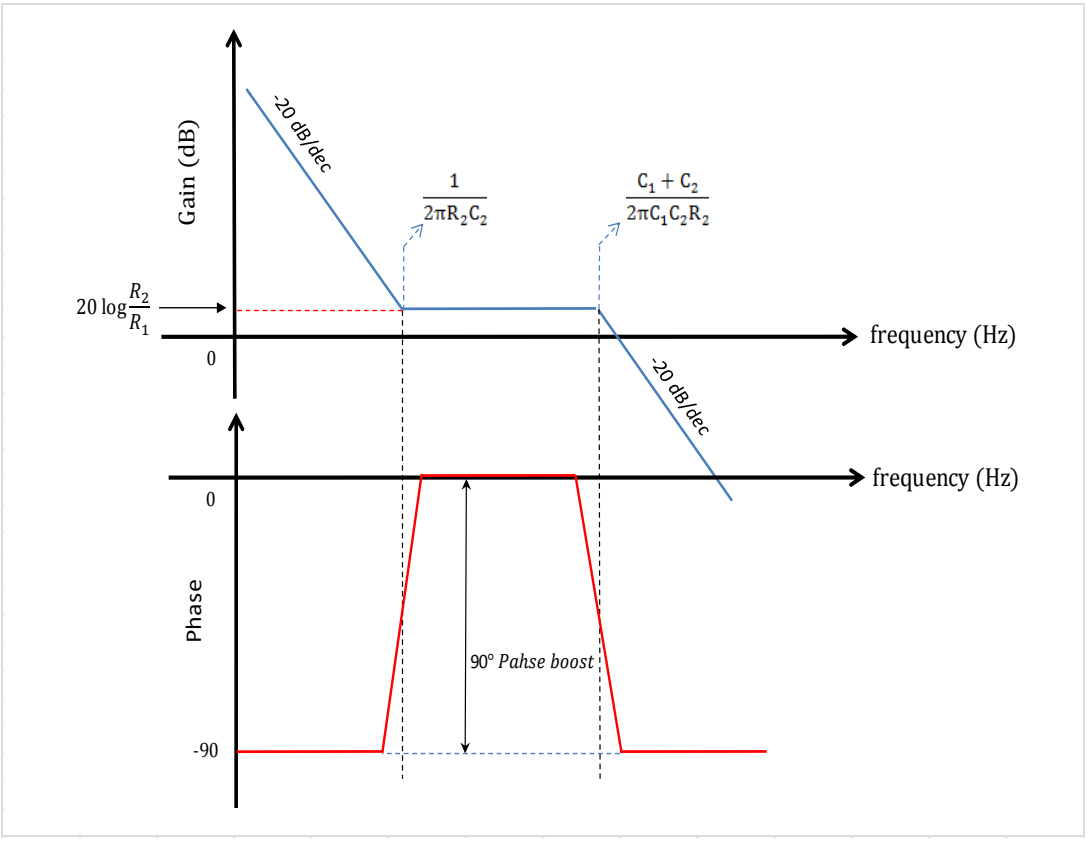

Figure 4.7 Bode plot of Type II compensator [18]

4.3.3 Type III compensator

The circuit of the type III compensator which is also called third-order integral-lead controller is depicted in figure 4.8;

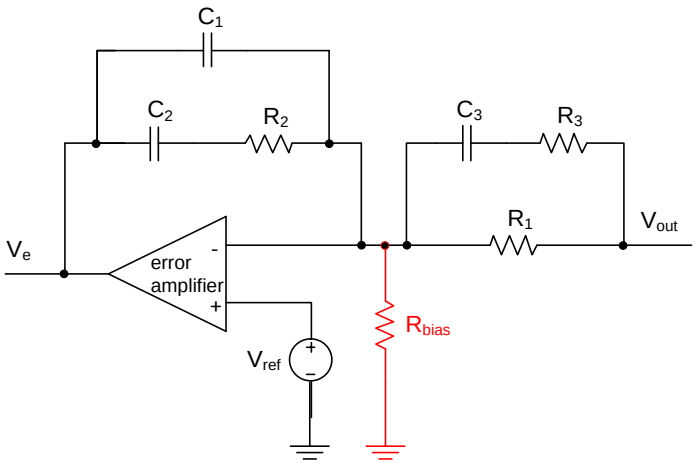

Figure 4.8 Type III compensation network [18]

As mentioned before when the phase boost provided by output filter's capacitor ESR in not sufficient (ESR value is small) type III compensator is useful to provide enough phase boost (theoretically 180 °) by adding an extra zero to the system's closed-loop transfer function.

4.3.3.1 Transfer function of type III compensator

The transfer function of type III compensator has a pole at origin and two zero-pole pairs. The capacitor C_1 and the series combination of the resistance R_1 and resistance R_3 provide a pole at the origin which form the integral part of compensator circuit. The capacitor C_2 and the resistance R_2 together introduce a zero and also the capacitor C_3 and the series combination of the resistance R_1 and resistance R_3 introduce the second zero. The resistance R_2 and the series combination of capacitor C_1 and the capacitor C_2 provide a pole. Finally the capacitor C_3 and the resistance R_3 introduce the second pole of the system [1].

As in type II compensator the integral part is employed to increase the gain of the system at low frequencies in order to reduce DC error, but since this part causes a phase lag -90 ° at all frequencies the lead compensator part is therefore used to reduce the phase lag. This is done by introducing two zeros to the transfer function of closed-loop system which leads to increase the gain crossover frequency and attain a faster transient response [1].

If we assume that error-amplifier is ideal the transfer function of type III compensator can be achieved from following equations:

$$\frac{V_{out}}{\left(R_3+\frac{1}{C_3 s}\right)||R_1} = -\frac{V_E}{\left(R_2+\frac{1}{C_2 s}\right)||\frac{1}{C_1 s}} \qquad (Eq.\,4.19)$$

From equation 4.19:

$$\frac{V_E}{V_{out}} = -\frac{R_1 + R_3}{R_1 R_3 C_1} \cdot \frac{\left(s + \frac{1}{R_2 C_2}\right)\left(s + \frac{1}{(R_1 + R_3)C_3}\right)}{s.\left(s + \frac{C_1 + C_2}{R_2 C_1 C_2}\right)\left(s + \frac{1}{R_3 C_3}\right)} \qquad (Eq.4.20)$$

As can be seen in equation 4.20, the transfer function of Type III has a pole at origin and two zero-pole pairs at frequencies;

$$f_{z_1 c_3} = \frac{1}{2\pi R_2 C_2} \qquad (Eq.4.21)$$

$$f_{z_2 c_3} = \frac{1}{2\pi (R_1 + R_3) C_3} \qquad (Eq.4.22)$$

$$f_{p_1 c_3} = \frac{C_1 + C_2}{2\pi R_2 C_1 C_2} \qquad (Eq.4.23)$$

$$f_{p_2 c_3} = \frac{1}{2\pi R_3 C_3} \qquad (Eq.4.24)$$

Figure 4.9 depicts the bode plot of the type III compensator which makes 180 ° phase boost due to two zeros [18]. (Practically less than160 °)

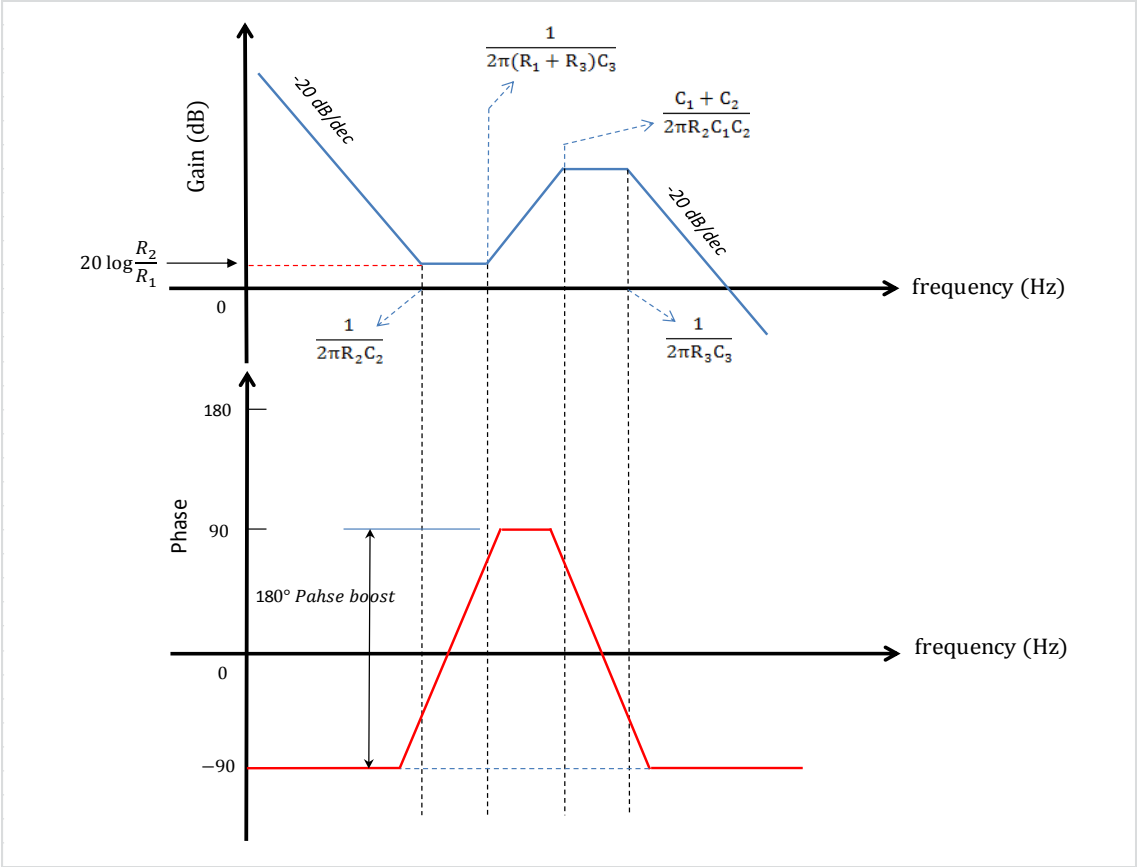

Figure 4.9 Bode plot of Type III compensator [18]

4.4 Feedback Control Loop

As mentioned before there are two main types of feedback control topology; current mode control and voltage mode control to regulate DC/DC converter's output voltage.

Assurance of the stability of the system and regulation of the output voltage by adjusting the switching duty cycle are two main goals of feedback control loop in the DC/DC converter. Commonly the feedback control part consists of two main components; voltage error-amplifier (with compensation circuit) and voltage comparator to keep close the output voltage to set reference voltage.

4.4.1 Current Mode Control (CMC)

As shown in figure 4.10, current mode control system has two control feedback loops: internal feedback loop that senses and controls inductor peak current which is called current loop and also external feedback loop that senses and regulates the output voltage which is called voltage loop.

The reason that this method is called current mode control is that it controls the inductor current directly via internal control loop, while the output voltage is regulated indirectly by the internal current loop. The basic idea of operation is that the internal current loop senses the inductor current then according to current changes through inductor it adjusts the duty cycle and the external voltage loop provides a reference voltage for the internal loop in response to changes in the output voltage, this process will continue until the output voltage be regulated [1].

4.4.1.1 Architecture

The internal current loop is included four main parts; current sensor, voltage comparator, SR latch and clock generator which controls the switching duty cycle.

As can be seen the inductor current i_L is sensed with resistance R_s as a current sensor and then voltage $R_s i_L$ applies to non-inverting input of voltage comparator. The comparator compares this voltage with control voltage V_c which is applied to its inverting input (generated by error-amplifier from the external voltage loop) when voltage $R_s i_L$ is higher than control voltage V_c (increase in i_L) the output comparator goes low but when voltage $R_s i_L$ is less than control voltage V_c (reduction in i_L) the comparator's output goes to high leads to reset the SR latch then Q goes to low state to turn on the HSS (PMOS switch power) for adjusting inductor current. The HSS remains in on state till the SR latch is set by clock generator [1].

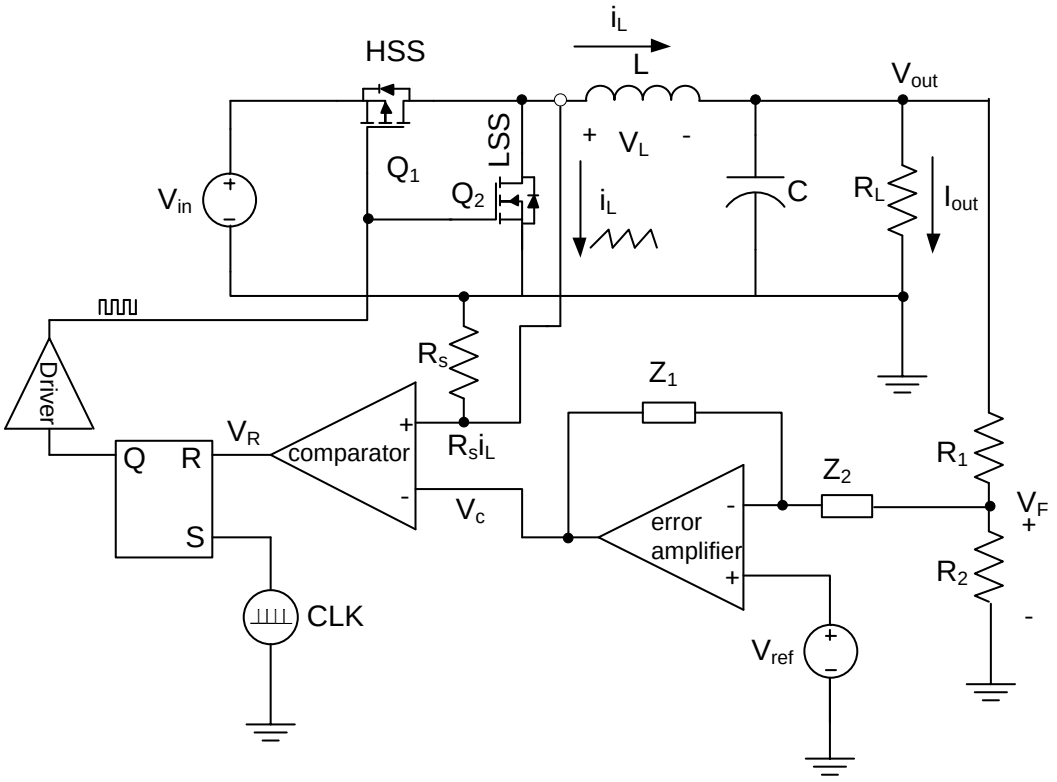

Figure 4.10 PWM Buck converter with current mode control (CMC) [1]

4.4.2 Voltage Mode Control (VMC)

As shown in figure 4.11, unlike the current mode control it has just one feedback loop which is called voltage control loop. Since the duty cycle is directly controlled by voltage reference V_{ref} and feedback voltage V_F via voltage loop this method is called voltage mode control.

4.4.2.1 Architecture

The voltage control loop usually contains two man parts: voltage error-amplifier and voltage comparator for regulating output voltage.

In this method the feedback voltage V_F is compared to reference voltage V_{ref} and their difference is amplified by error-amplifier which is appeared as voltage error V_e at the output of amplifier. Then this voltage error which is applied to non-inverting input of voltage comparator is compared to saw-tooth wave V_{saw} which is applied to inverting input of comparator in order to generate square pulses for controlling switching duty cycle, when the voltage error V_e is higher than V_{saw} the comparator output goes high whereas if the V_e is lower than V_{saw} its output goes low to adjust the switching duty cycle.

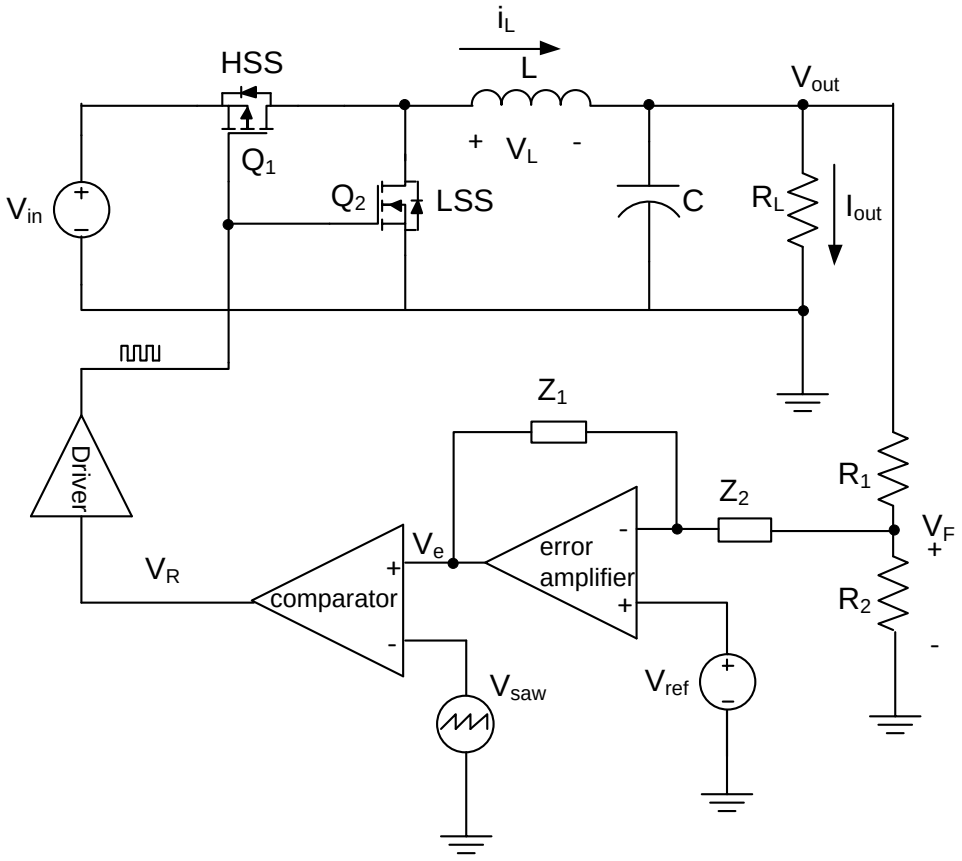

Figure 4.11 PWM Buck converter with voltage mode control (VMC) [1]

4.5 VMC vs. CMC

The important advantages and disadvantages of employing voltage mode or current mode control are mentioned as below:

- Since current mode control employs two feedback loops, controlling the output voltage of converter is easier than voltage mode control which uses just one voltage feedback loop. The extra loop (internal current control loop) makes an improvement in phase margin and stability and it does not need so much complicated circuit for phase compensation, usually type II compensation is enough and it makes the design of converter simpler however type III compassion is needed for voltage control mode to improve the phase margin of converter.
- Voltage control mode has different characteristics when moving from continuous conduction mode to discontinuous conduction mode so designing a compensation circuit that can operate properly in both modes is impossible while current mode control has almost the same characteristics in both CCM and DCM mode.
- Since in CMC the inductor current should be sensed it needs extra circuitry (current sensor) which causes power loss and complexity of system.
- If the duty cycle of converter is around 50% it can cause instability in current mode control [7].

- Noise and spikes on the current sense signal is one of the major issues in CMC and obtaining smooth ramp from sensed signal is not simple so inevitably sometimes filter is added to current sensor circuit to suppress the noise and spikes [7]. Figures 4.12 and 4.13 show the different between ideal current-sensed and real current-sensed signal's waveforms respectively.

Figure 4.12 Ideal current-sensed waveforms [7]

Figure 4.13 Practical circuit current-sensed waveforms [7]

4.6 Pulse Width Modulation (PWM)

Pulse width modulation which is called also duty cycle modulation is a technique for delivering the power to the load by using sequential fixed rectangular pulses based on reference voltage and error voltage [8]. Depending on how much power we want to deliver to the load the duty cycle of PWM waveform varies, for example figure 4.14.a (10% duty cycle) and figure 4.14.c (90% duty cycle) illustrate low power and high power delivering respectively.

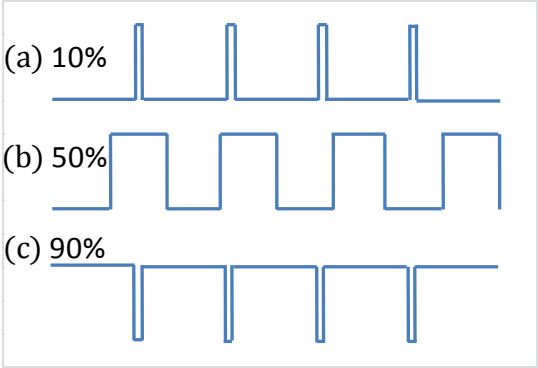

Figure 4.14 PWM signal with different duty cycles

Since in this technique the frequency is constant the switching noise is relatively low thus simple low-pass filter can be used to suppress the output voltage ripples properly.

4.7 Pulse Frequency Modulation (PFM)

PFM (also called power save mode 'PSM') is similar to PWM control method but instead of fixed frequency pulses it employs 'constant time variable frequency' to control delivering supply power to the load [8].

Figure 4.15 depicts the pulse frequency modulation for three different levels of load current.

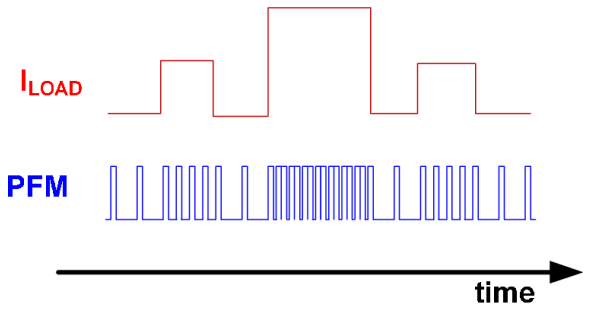

Figure 4.15 PFM signal with respect to load current variation [8]

When the load current is low instead of PWM technique this method is useful to increase the power efficiency of converter.

4.7.1 The structure of PFM control in buck converter

As shown in figure 4.16, in this technique first the feedback voltage V_F is compared to reference voltage V_{ref} by means of a voltage comparator, if V_F is lower than reference voltage then the signal V_{PFM} will goes low (by setting the SR flip-flop) to turn on PMOS power switch and turn off NMOS switch. The inductor current ramps up linearly while the PMOS switch conducts. When the inductor current reaches to the specified peak current (threshold current), the current comparator turns off PMOS switch and turns on NMOS switch (by resetting the SR flip-flop) to decline the peak current. On the other hand the zero-current detector is employed to turn off the NMOS switch when the inductor current goes to zero; therefore it avoids energy dissipation in the NMOS transistor caused by reverse flow of inductor current.

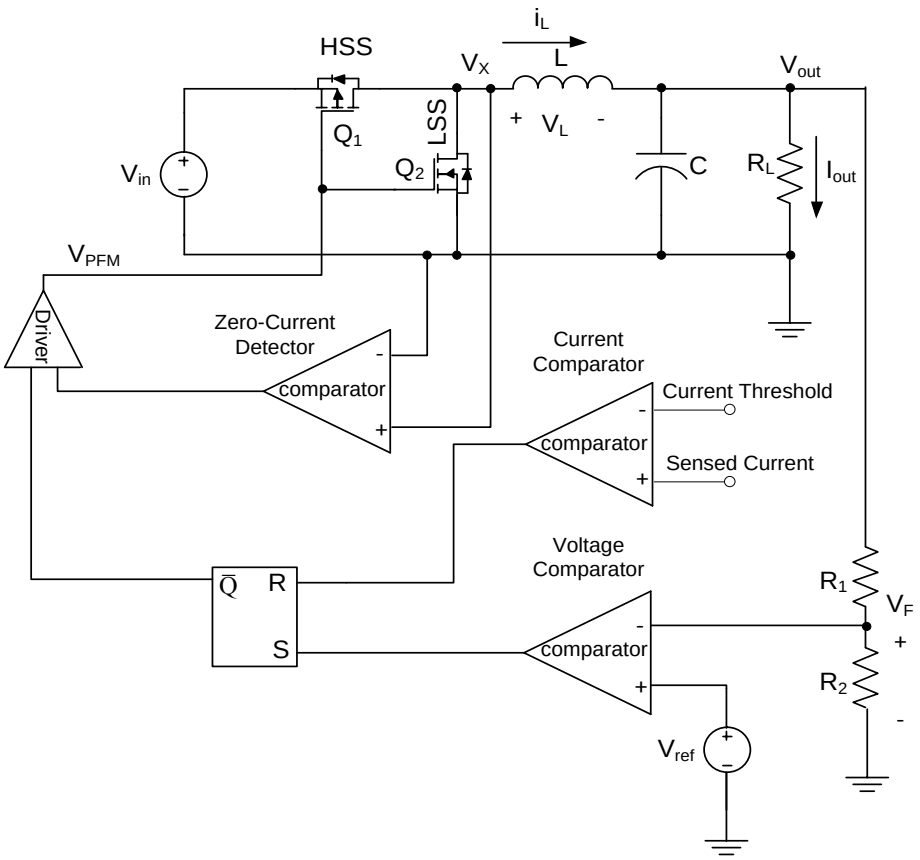

Figure 4.16 Structure of PFM control [31]

4.8 PFM vs. PWM

- PWM technique is efficient for moderate to high output power (high load current) where the duty cycle is longer but if this technique is used for low load current the efficiency of converter drastically reduces because the switching loss will dominate the total loss of converter circuit so instead, PFM method is employed to increase the converter's efficiency significantly.
- In PWM method due to the use of a fixed frequency the switching noises and the output voltage ripples are relatively low comparison to PFM technique which employs variable frequency, so with a simple low-pass filter the output voltage ripples caused by switches can be removed.
- PFM controlling circuit is more complex than PWM circuit and it has high electromagnetic interface (EMI) that is why the power supply designers usually avoid using it [8].
- PWM is frequency band limited whereas PFM has variable frequency band.

4.9 Continuous Conduction Mode vs. Discontinuous Conduction Mode

Buck converter can operate in two modes regarding the inductor's current wave form; CCM (Continuous Conduction Mode) and DCM (Discontinuous Conduction Mode). In continuous conduction mode, inductance current never falls to zero during discharge interval but in DCM mode due to low load current, the inductor current falls to zero and remains in this state until charging cycle of inductor.

Figures 4.17 and 4.18 show the inductor current waveform for synchronous (which NMOS is used as a LSS) and asynchronous (which diode is used as a LSS) buck converter respectively in both low output current and high output current [9].

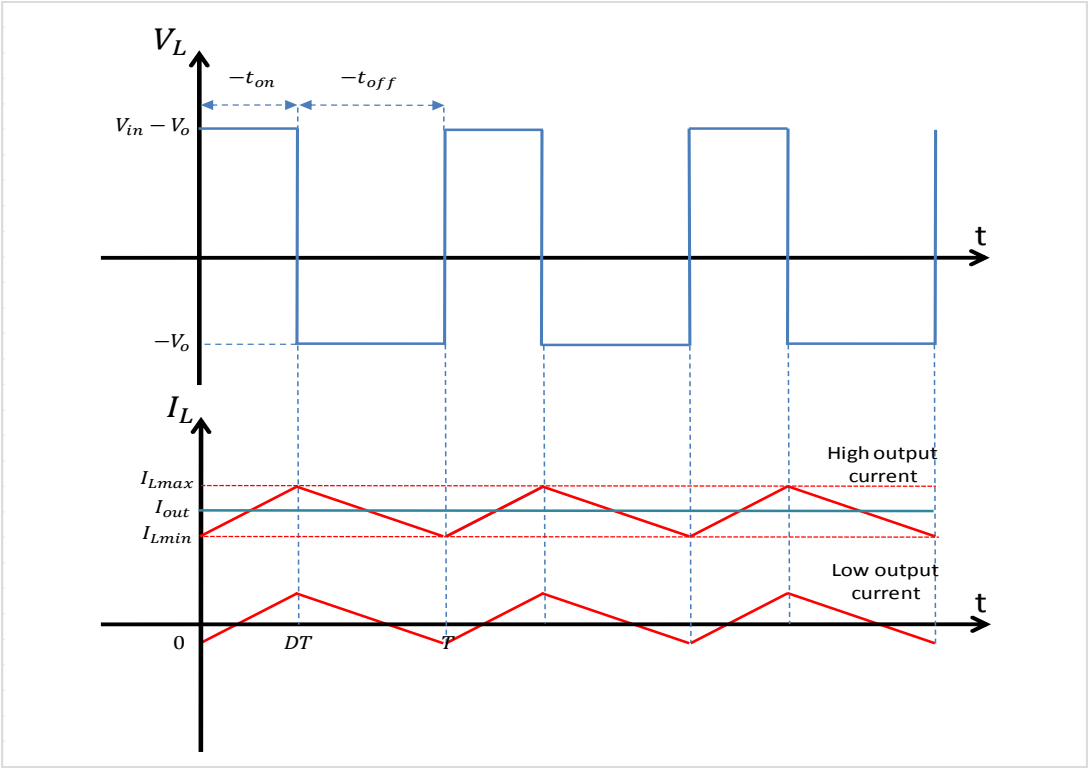

Figure 4.17 Inductor current waveform in a synchronous buck converter [9]

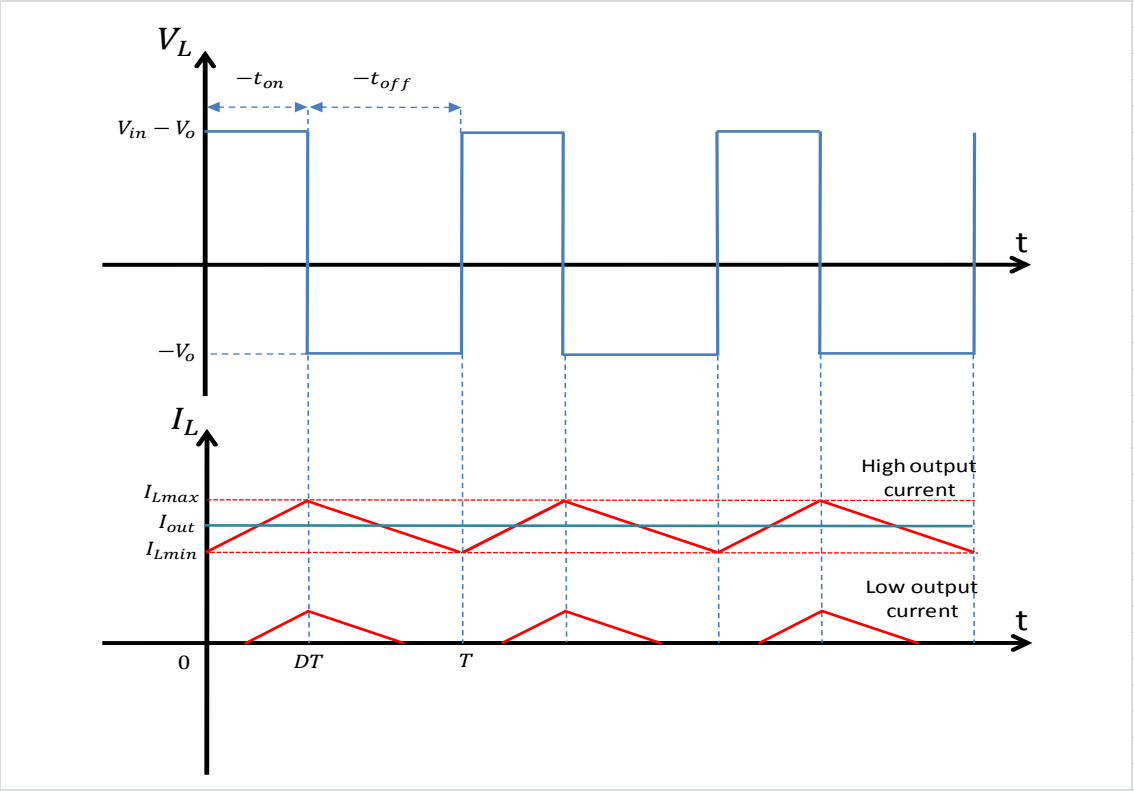

Figure 4.18 Inductor current waveform in an asynchronous buck converter [9]

As can be seen both asynchronous buck converter and synchronous buck converter maintain in CCM operation mode when output load current is high, but since in synchronous buck, MOSFET is employed instead of external diode thus it losses less power than asynchronous buck. Therefore it will be more efficient if we use synchronous buck instead of conventional buck for high output current.

The story is different when the output current is low. For low output current, asynchronous buck converter goes to DCM mode operation since diode is current-unidirectional switch so it blocks the negative current but since MOSFET is current-bidirectional switch thus negative current can flow through it and it will not be blocked. So it maintains in CCM mode, therefore it would be more efficient if we use asynchronous buck instead of synchronous for very low output current because during a period that diode is in zero volt there is no conduction loss and does not dissipate any power [9].

Chapter 5

Design and performance evaluation of buck converter

5.1 DC/DC buck converter's specifications

There are so many factors should be taken into account for designing DC/DC converters like power efficiency, transient response, settling time, output voltage ripples, stability of system and occupied area in the chip. For instance faster transient response can be achieved by increasing frequency but on the other hand higher frequencies causes lower efficiency therefore always there is trade-off between transient response of the system and efficiency of converter.

The specification for designing the DC/DC buck converter is according to table 5.1;

Technology	65 nm CMOS process
Input Voltage	1.1 v
Output Voltage	500 mV
Output current range	< 1mA
Output Power	400µW
Switching Frequency	20 MHz
Allowed voltage ripple (percentage)	1%
Allowed current ripple(peak to peak)	1 %
Minimum efficiency	70 %
Output capacitor ESR	75mΩ
Inductor DCR (DC resistance)	50mΩ

Table 5.1 Buck converter specifications

5.2 Buck converter's circuit

The Most DC/DC buck converters replace their freewheel diode (which is used in conventional converters) with a NMOS transistor in order to increase the efficiency of converter in the low output voltage condition and make the fully integration of the power switches on chip. There is however a disadvantage of this replacement because it is low efficient in very light load due to conduction of NMOS switch during the whole discharge cycle. Therefore, when the converter works in very light load, i_L is discharged down to zero and begins to flow from the output V_{out} to ground through the turned on NMOS transistor

(bidirectional switch), on the other hand synchronous buck converter always works in CCM mode in very light load (figure 4.17), result in great energy consumption in very low load condition.
To have a synchronous buck converter with high performance and efficiency over a wide range of load current, it should be able to operate also in DCM mode for very low loads, Like [31] and [32] which inductor current below zero will be canceled by using different control techniques, so that the efficiency under very light-load will be greatly increased.

There are so many other control techniques to improve the efficiency of buck converter in the both light and heavy loads, but since in this thesis during discharging interval the inductor current never goes below zero (in the desired voltage range) therefore there is no need to employ complicated feedback topology to control CCM or DCM mode of the system. On the other hand the buck converter is designed for ultra-low power application in the range of μwatt, adding any extra blocks and components in the feedback control loop of the circuit will consume so much energy and therefore the total efficiency of converter will be drastically reduced. Thus in this work it is preferred to use simple but efficient Voltage Mode Control loop to keep the overall performance in good condition. Figure 5.1 shows the designed buck converter circuit:

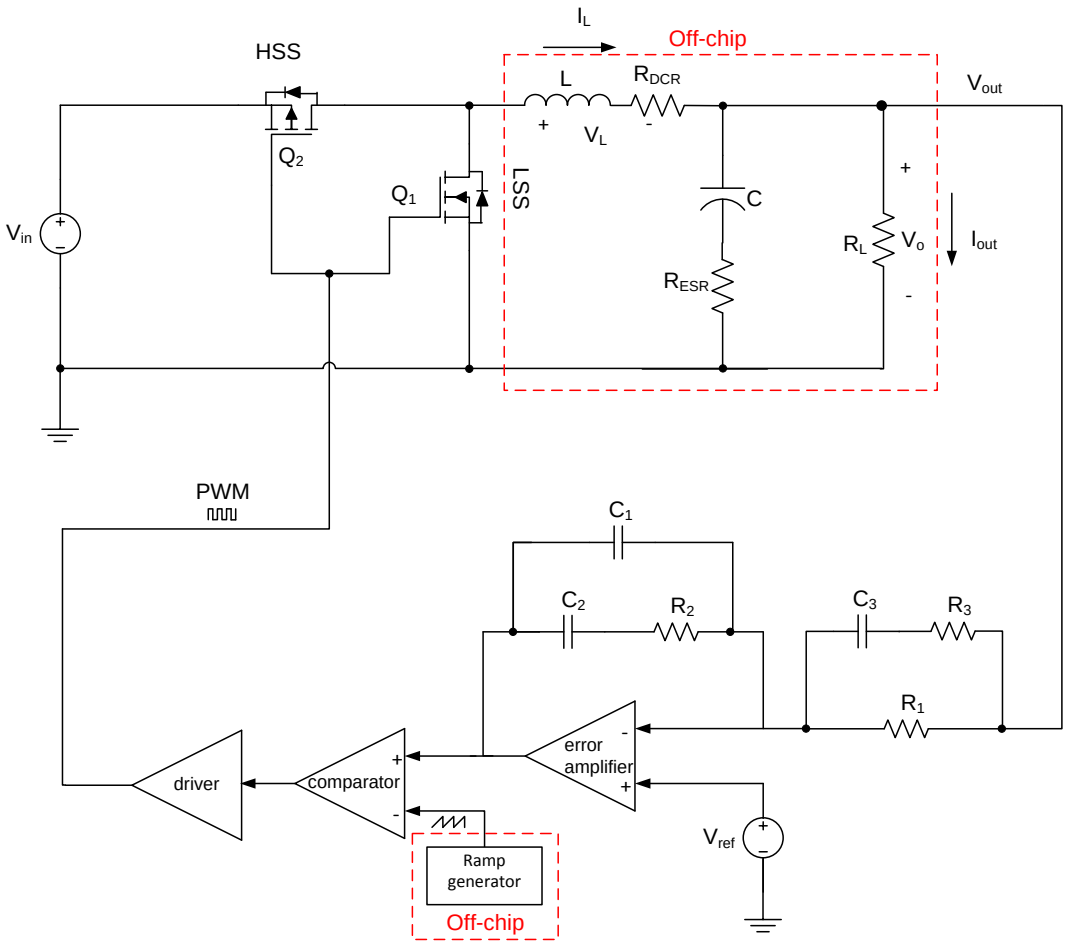

Figure 5.1 Buck converter's circuit

All transistors in the circuit downsized to reduce the area of chip, the power MOSFETs are chosen to have a low on resistance R_{DSon} to reduce the conduction losses and low gate-charge to reduce switching losses. (HSS Q_2 (PMOS) and LSS Q_1 (NMOS) sized 7 µm and 6.3 µm respectively). The operation frequency of converter is chosen high enough (20MHz) in order to reduce the size of output filter's inductor and capacitor and simultaneously have a desired efficiency. The higher frequency operation allows the on-chip integration of filter capacitor and inductor but the problem is that converter's efficiency dramatically will be reduced due to higher power loss, therefore to meet the converter's specifications the operation frequency 20 MHz is chosen.

5.3 Parameters' calculation:

5.3.1 Calculation of minimum value of inductor and output filter capacitor

5.3.1.1 Inductor size

The values of inductor and capacitor of the output filter are the first elements that should be calculated in designing a DC/DC buck converter. The minimum value of inductor is calculated based on the following equations:
The inductor current i_L can be measured according to Faraday's law (Eq.5.1):

$$V_L = L\frac{dI_L}{dt} \qquad (Eq.5.1)$$

For $0 < t \leq D.T$;

$$i_L = \frac{V_i - V_o}{L}t \qquad (Eq.5.2)$$

Where V_i input voltage and V_o is output voltage of buck converter.
The inductor current waveform at the boundary between CCM and DCM operation is shown in figure 5.2:

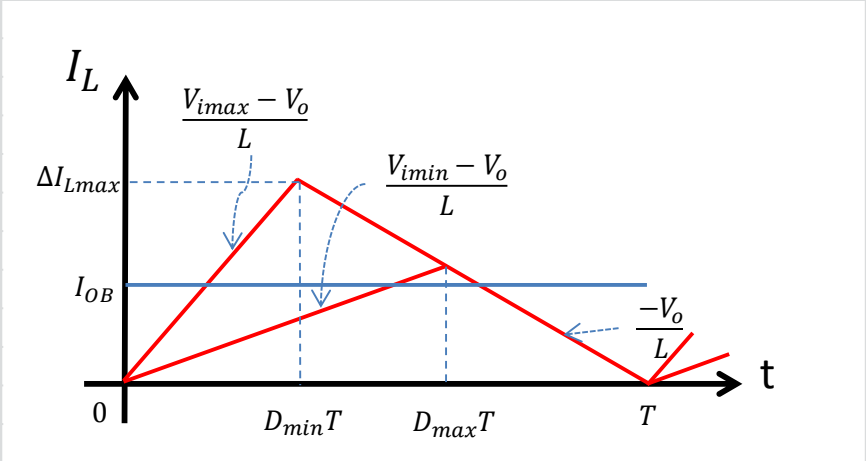

Figure 5.2 Inductor current waveform at the CCM/DCM boundary [1]

The peak current at boundary can be express in equation 5.3:

$$\Delta i_L = i_L(DT) = \frac{(V_i - V_o)}{L}D.T = \frac{V_o(1-D)}{L.f_s} \qquad (Eq.5.3)$$

The maximum Peak-to-peak of inductor ripple current can be obtained from equation 5.4;

$$\Delta i_{Lmax} = \frac{V_o(1-D_{min})}{L_{min}.f_s} \qquad (Eq.5.4)$$

Thus the minimum inductor value which is needed in buck converter to operate in the continues current mode for $D_{min} \leq D \leq D_{max}$ can be achieved from equation 5.5 [1]:

$$L_{min} = \frac{V_o(1 - D_{min})}{f_s \Delta i_{Lmax}} \qquad (Eq. 5.5)$$

Based on the specifications below:

$$\begin{cases} V_{out} = 500mv \\ V_{in\_max} = 1.4\ v \\ D_{min} = \dfrac{V_{out}}{V_{in\_max}} = \dfrac{0.5}{1.4} \simeq 0.36 \\ \Delta i_{Lmax} = 5mA \\ f_s = 20MHz \end{cases}$$

The minimum inductor's size is calculated from equation 5.6:

$$L_{min} = \frac{V_o(1 - D_{min})}{f_s \Delta i_{Lmax}} = \frac{0.5(1 - 0.36)}{20MHz.5mA} = 3.2\mu H \qquad (Eq. 5.6)$$

As we can see inductor size is inversely proportional with switching frequency in other words by increasing the switching frequency we can reduce the size of inductor which yields decrease in total circuit area. But there is a tradeoff between size of inductor and switching frequency because when the switching frequency increases, the power loss in the power switches increases, so that the converter's power efficiency declines. Also when the size of inductor reduces, inductance current ripple growths up which is not desired, because increase in inductor current ripple leads to increase voltage ripple at the output of system therefore In this work in order to limit the peak-to-peak current ripples and reduce the power loss in inductor and power MOSFETs, the inductor size is chosen a bit larger than calculated one to meet the performance specifications;

Preferred size of inductor: 8.5 μH

Figure 5.3 shows the transient response of inductor's peak-to-peak current ripple (Δi_L) and the load current I_o which is equal to average of Δi_L;

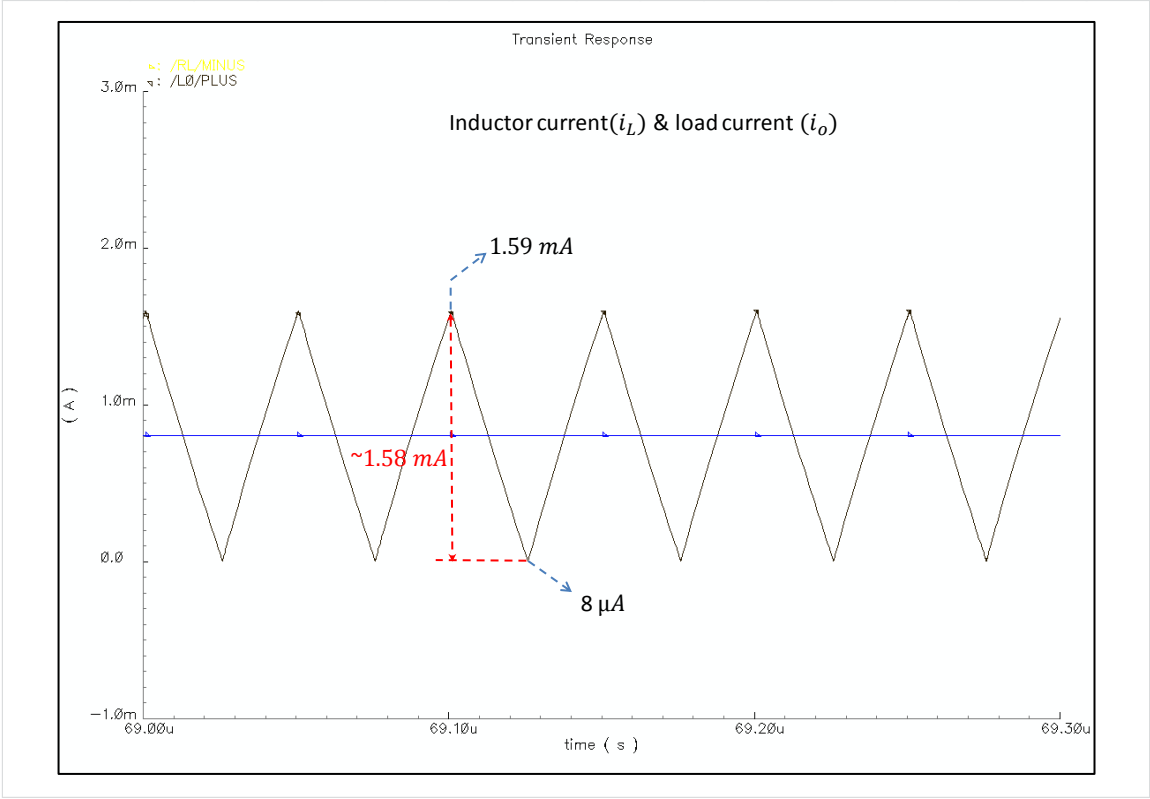

Figure 5.3 Inductor and load current waveform

5.3.1.2 Capacitor size

The minimum size of capacitor which is required to overcome the output voltage ripple can be determined according to following procedure:

First we assume that we are in off state (DT <t≤ T) it means that HSS (S_1) is off and switch LSS (S_2) is on, thus energy which is stored in inductor L starts to discharge through S_1 to the load and capacitor C.

Figure 5.4 shows that the waveform of current flow through load capacitor C is the same with inductor current, (same ripple size) just its level is lower than inductor current. The maximum increase of the charge (ΔQ) which is stored in filter capacitor C is equal to striped triangle area therefore by calculation the striped area we can obtain ΔQ for each cycle from equation 5.7:

$$\Delta Q = \frac{1}{2}\frac{T}{2}\frac{\Delta i_{Lmax}}{2} = \frac{T\Delta i_{Lmax}}{8} = \frac{\Delta i_{Lmax}}{8f_s} \qquad (Eq.5.7)$$

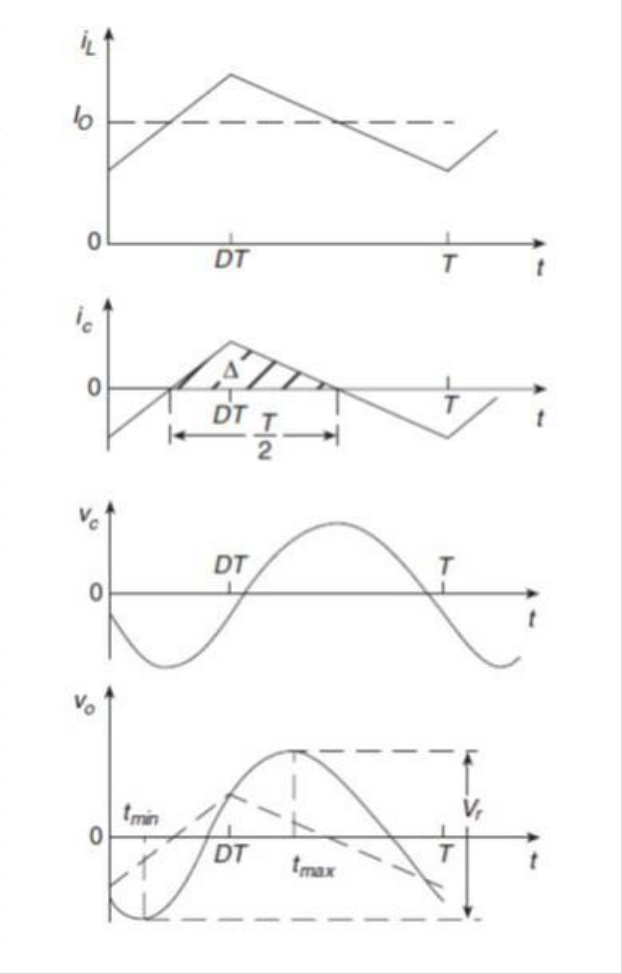

Figure 5.4 Voltage ripple waveforms of the buck converter [1]

The peak to peak voltage ripple across the filter capacitor is expressed in equation 5.8:

$$V_{Cpp} = \frac{\Delta Q}{C} = \frac{\Delta i_{Lmax}}{8 f_s C} \qquad (Eq. 5.8)$$

From the equation 5.4:

$$V_{Cpp} = \frac{V_o(1 - D_{min})}{8LC.{f_s}^2} \qquad (Eq. 5.9)$$

Since the double pole frequency of output filter is equal to:

$$f_{LC} = \frac{1}{2\pi\sqrt{LC}} \qquad (Eq. 5.10)$$

Thus we can calculate the peak to peak voltage ripple across the capacitor C in terms of double pole frequency from equation 5.11:

$$V_{Cpp} = \frac{V_o(1 - D_{min})\pi^2 {f_{LC}}^2}{2{f_s}^2} \qquad (Eq. 5.11)$$

So the minimum size of capacitor for output filter to reduce the peak to peak voltage ripple is achieved from equation 5.12:

$$C_{min} = \frac{\Delta i_{Lmax}}{8 f_s V_{Cpp}} = \frac{V_o(1 - D_{min})}{8 L {f_s}^2 V_{Cpp}} \qquad (Eq. 5.12)$$

As we can see capacitor size is inversely proportional to square value of switching frequency, therefore by increasing the switching frequency we can reduce the size of filter capacitance but on the other hand we should consider that increase in switching frequency leads to drop in converter's power efficiency [1].

To determine the value of output filter capacitor we assume the worst case ($D_{min} = 0$ or $D_{max} = 1$), thus according to equation 5.12 the minimum value of output filter capacitor is determined from following calculation;

Assumption; $V_{Cpp} = 0.1mv$ (Voltage ripple across the capacitance C)

$$C_{min} = \frac{\Delta i_{Lmax}}{8 f_s V_{Cpp}} = \frac{5mA}{8 \times 20MHz \times 0.1mv} = 312.5\ nF \qquad (Eq. 5.13)$$

For safety 330 nF is preferred for output filter capacitance.

5.4 Method for choosing type II or type III compensation

The following procedure is employed to select which compensation type is suitable and easier for implementation for regulating the output voltage properly:
If ESR of the output filter capacitance is low so that f_{ESR} is equal to or greater than 5 times of output filter's double pole frequency f_{LC} then type III compensation is employed to meet the stability criteria by adding extra zero to the system's closed-loop phase, but when ESR value is high so that f_{ESR} is less than 5 times of f_{LC} then type II compensation is enough to have a sufficient phase margin [20].
The equivalent series resistance zero frequency is expressed in equation 5.14:

$$f_{ESR} = \frac{1}{2\pi . ESR . C_o} \qquad (Eq. 5.14)$$

From the specification ESR=75mΩ, therefore according to equation 5.14 the ESR zero frequency is calculated:

$$f_{ESR} = \frac{1}{2\pi . 75m\Omega . 330nF} \simeq 6.43MHz \qquad (Eq. 5.15)$$

By comparing ESR zero frequency f_{ESR} and output filter's double pole frequency f_{LC} which is calculated according to equation 5.10:

$$f_{LC} = \frac{1}{2\pi\sqrt{8.5\mu H.330nF}} \simeq 95KHz \qquad (Eq.5.16)$$

We can see that f_{ESR} is much higher than f_{LC} thus based on above procedure, type III compensation is employed to have a sufficient phase boost at the closed-loop system.

5.5 Type III compensator's components value

For positioning the poles and zeros at the desired places to have enough phase margin the components value of type III compensator is calculated according to following procedure:

- Assumption: $R_1 = 2k\Omega$ and DBW (Desired Bandwidth) = 6MHz (30% switching frequency)
- To have a desired bandwidth the ratio of R_2/R_1 (type III error amplifier gain in horizontal part of its transfer function [4]) should be large enough. This will be accomplished by calculating R_2 from equation 5.17:

$$R_2 = \frac{DBW}{f_{LC}}.\frac{\Delta V_{saw}}{V_{in}}.R_1 \qquad (Eq.5.17)$$

- Placing the first zero at the half of the output filter double pole frequency, it will be accomplished by calculation C_2 from equation 5.18:

$$C_2 = \frac{1}{\Pi\, R_2 f_{LC}} \qquad (Eq.5.18)$$

- Set the first pole at the ESR zero frequency which will be done by calculation C_1 from equation 5.19:

$$C_1 = \frac{1}{(2\Pi\, R_2 C_2 f_{ESR}) - 1} \qquad (Eq.5.19)$$

- Placing the second pole at 50% of switching frequency and also set the second zero at the output filter double pole frequency, it will be accomplished by calculation R_3 and C_3 from following equations:

$$R_3 = \frac{R_1}{\left(\frac{f_{sw}}{2f_{LC}}\right) - 1} \qquad (Eq.5.20)$$

$$C_3 = \frac{1}{\Pi\, R_3 f_{sw}} \qquad (Eq.5.21)$$

Table 5.2 shows the calculated components value according to the above procedure;

R_1	2kΩ
R_2	57kΩ
R_3	19Ω
C_1	434fF
C_2	58pF
C_3	829pF

Table 5.2 Type III compensator's calculated components

Based on the calculated values the total open loop gain of the buck converter and the output filter's gain are plotted in cadence, as shown in figure 5.5:

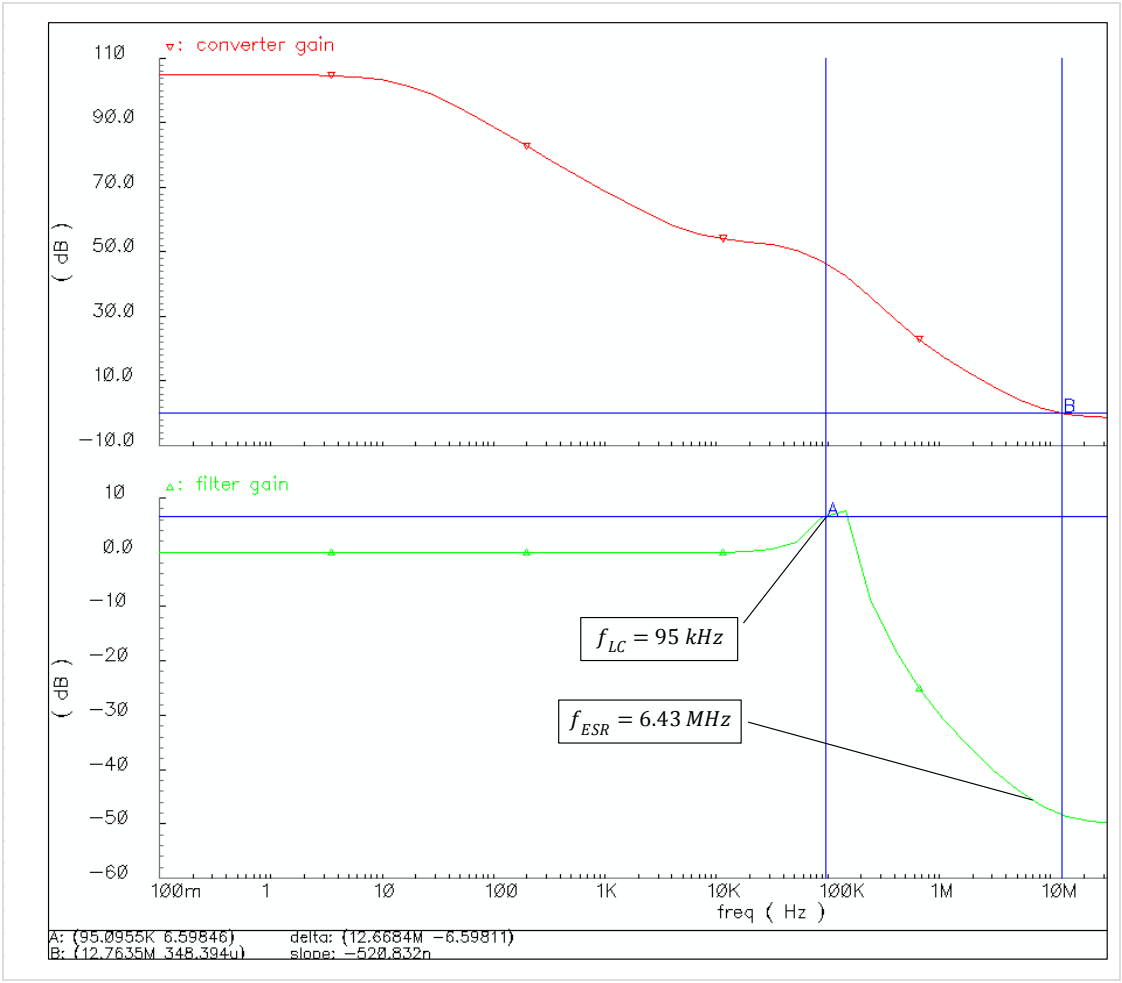

Figure 5.5 Converter and output filter's gain plot

5.6 Variations in output voltage and output current ripples with different sizes of filter capacitor

Table 5.3 shows the effect of different values of output filter capacitor C on output voltage and load current ripples. As can be seen when the output capacitance is reduced from 330 nF to 55 nF (6 times reduction) both the output voltage and load current ripples increase drastically.

C_o	330nF	82.5nF	55nF	41.25nF
L	8.5 µH	34 µH	51 µH	68 µH
RL	625Ω	625Ω	625Ω	625Ω
Input Voltage	1.1v	1.1v	1.1v	1.1v
Average Output Voltage	504mV	504mV	504.9mV	506.5mV
Output Current	806.4µA	806.4µA	807.9µA	810.4µA
Average Output power	406.4µW	406.4µW	407.9µW	410.5µW
Average input power	485.6µW	473.7µW	488.1µW	464.4µW
Switching Frequency	20MHz	20MHz	20MHz	20MHz
voltage ripple(peak to peak)	0.12mV	0.1mV	8.05mV	14.15mV
current ripple(peak to peak)	0.2µA	0.15µA	12.89µA	22.6µA
Settling time	45.8µs	15.2µs	12.9µs	12.3µs
Power efficiency (%)	83.68%	85.8%	83.58%	88.39%

Table 5.3 Effect of different sizes of filter capacitor on output voltage and current ripples

5.7 Error amplifier schematic and its open-loop simulation result

Two-stage amplifier is chosen as an error amplifier to provide enough gain and phase margin. As shown in figure 5.6 the amplifier is included the differential input pair, current mirror and output stage. One of the amplifier's differential inputs is connected to reference voltage V_{ref} and another one is connected to feedback voltage V_F which is taken from the output of buck converter and their amplified difference is appeared at the output of amplifier.

The differential input pair transistors (M_1 and M_2) and transistor M_8 are sized to have a high gm which yields a high voltage gain. High gain is needed to improve the voltage regulation by keeping the difference between the reference voltage and feedback voltage small (smaller error voltage) [21]. The biasing current is chosen a small value (approximately 12.5 µA) to reduce the power losses in the control loop of the system. This error amplifier can work properly in the system in the range of 100 mV to 700 mV.

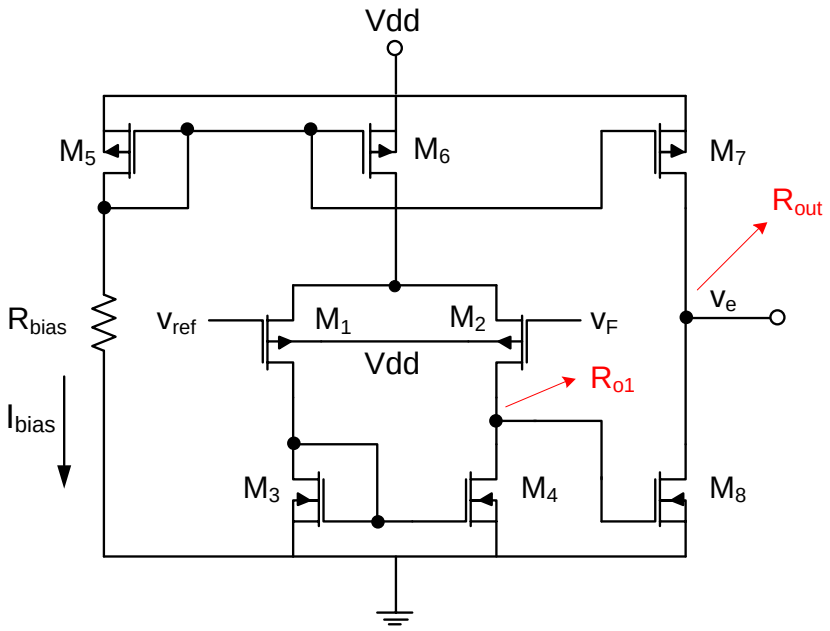

Figure 5.6 Error amplifier schematic

Small signal gain of amplifier can be calculated from equation 5.22:

$$G = gm_2 . gm_8 . R_{o1} . R_{out} \qquad (Eq. 5.22)$$

Which R_{o1} and R_{out} are output impedance of the first and second stages respectively which are obtained from equations 5.23 and 5.24;

$$\begin{cases} R_{o1} = r_{o2} || r_{o4} = \dfrac{1}{gds_2 + gds_4} & (Eq. 5.23) \\ R_{out} = r_{o7} || r_{o8} = \dfrac{1}{gds_7 + gds_8} & (Eq. 5.24) \end{cases}$$

$$G = \frac{gm_2 . gm_8}{(gds_2 + gds_4).(gds_7 + gds_8)} \qquad (Eq. 5.25)$$

From cadence simulation;

$$\begin{cases} gm_2 = 254.1\ \mu \\ gm_8 = 80.7\ \mu \\ gds_2 = 5.9\ \mu \\ gds_4 = 2.8\ \mu \\ gds_7 = 2.1\ \mu \\ gds_8 = 186.7\ n \end{cases} \longrightarrow \boxed{\text{G= 60.26 dB}}$$

Figure 5.7 depicts the open-loop gain and phase of error amplifier. Simulation result shows that the phase margin, DC-gain and unity-gain frequency (Fu) are 75.59°, 61.13 dB and 43.09 MHz respectively.

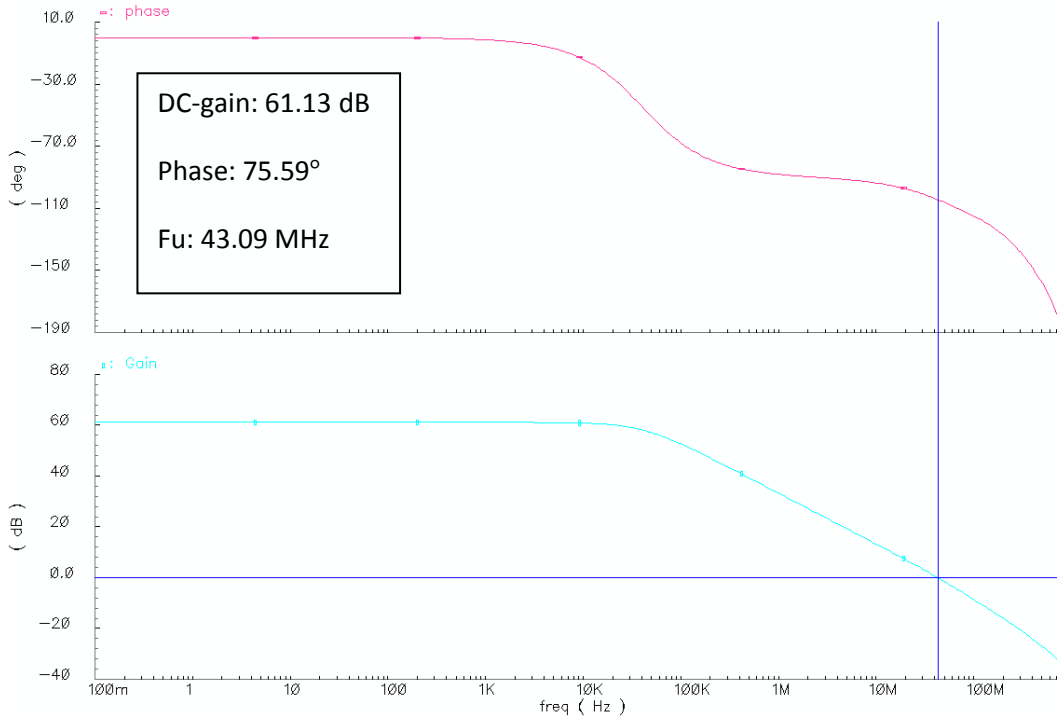

Figure 5.7 Open-loop Bode Plot of error amplifier

5.8 Comparator and driver schematic and their simulation results

Comparator schematic is chosen similar to error amplifier but since we don't need to get more voltage gain from comparator so only the sizing of transistors is different (smaller) and since it does not need the amplifier's compensation network, it is quite faster.

As shown in figure 5.1 the sawtooth ramp is applied to inverting input of comparator and the error signal which is coming from output of error amplifier is applied to non-inverting input to be compared with sawtooth wave to generate pulse width modulation (PWM) wave at the output of comparator in the feedback loop of the buck converter.

To obtain a smoother PWM waveform for driving the power transistors properly, a driver is connected at the output stage of comparator, figure 5.8 shows the driver schematic which is included four simple inverter stages with proper sizing of transistors to achieve a desired square-wave signal which yields reduction in power consumption at power stage of the system:

$$\left(W/L\right)_6 = 1.25 \times \left(W/L\right)_4 = 2.5 \times \left(W/L\right)_2 = 5 \times \left(W/L\right)_0$$

$$\left(W/L\right)_7 = 1.33 \times \left(W/L\right)_5 = 2 \times \left(W/L\right)_3 = 4 \times \left(W/L\right)_1$$

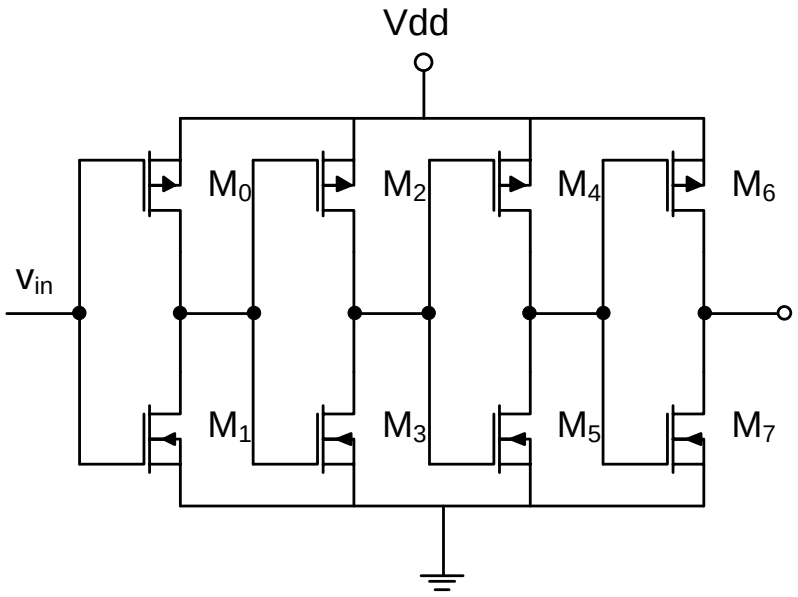

Figure 5.8 Driver schematic

Figure 5.9 shows the transient response simulation results of comparator (with driver), power switches' on-off state and output voltage waveforms:

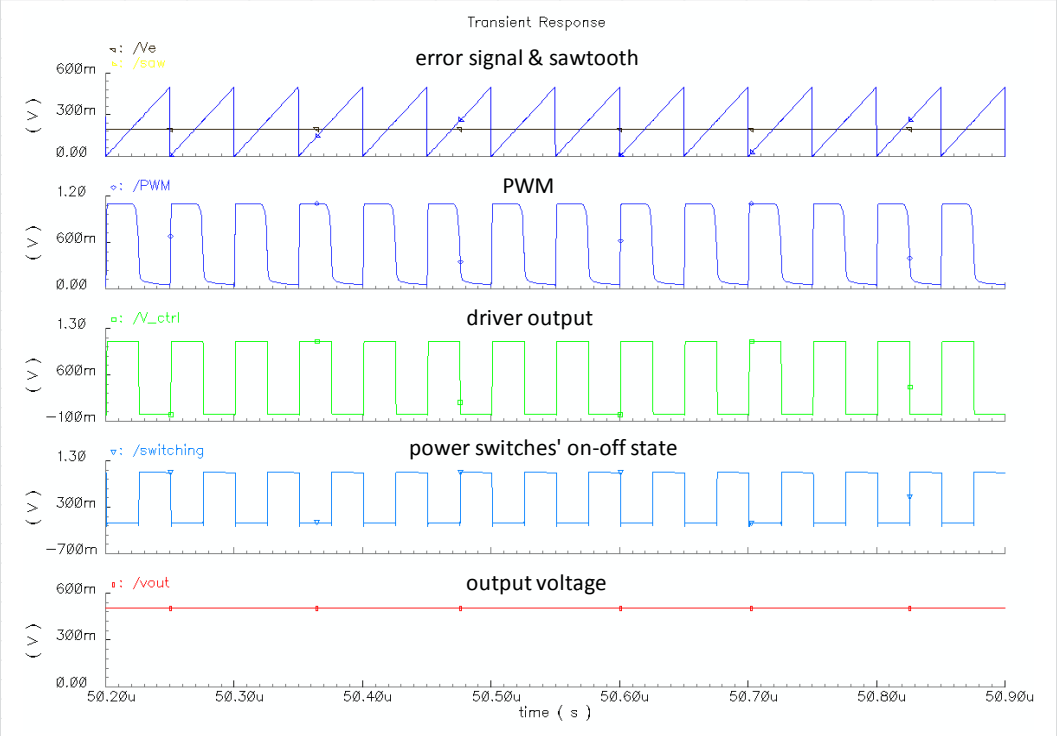

Figure 5.9 Simulation results

5.9 Effect of ESR and DCR on filter characteristic

Figures 5.10 and 5.11 show the effect of the parasitic resistances (ESR and DCR) on the phase and gain characteristic of output filter which depends on their value on the circuit and we cannot conclude from this discussion that lossy elements cause an increasing gain and phase characteristics of filter in all cases [14].

As can be seen the phase and the gain response of filter is changed when the parasitic resistances are included to the output capacitor and inductor. For instance since ESR provides a zero at the transfer function of lossy filter thus the gain slope of the output filter is increased +20 dB (from -40 dB to -20 dB) at f_{ESR} frequency but since there is no parasitic resistance in lossless filter the gain plot has a sharp slope (-40 dB) above LC cutoff frequency due to double pole frequency.

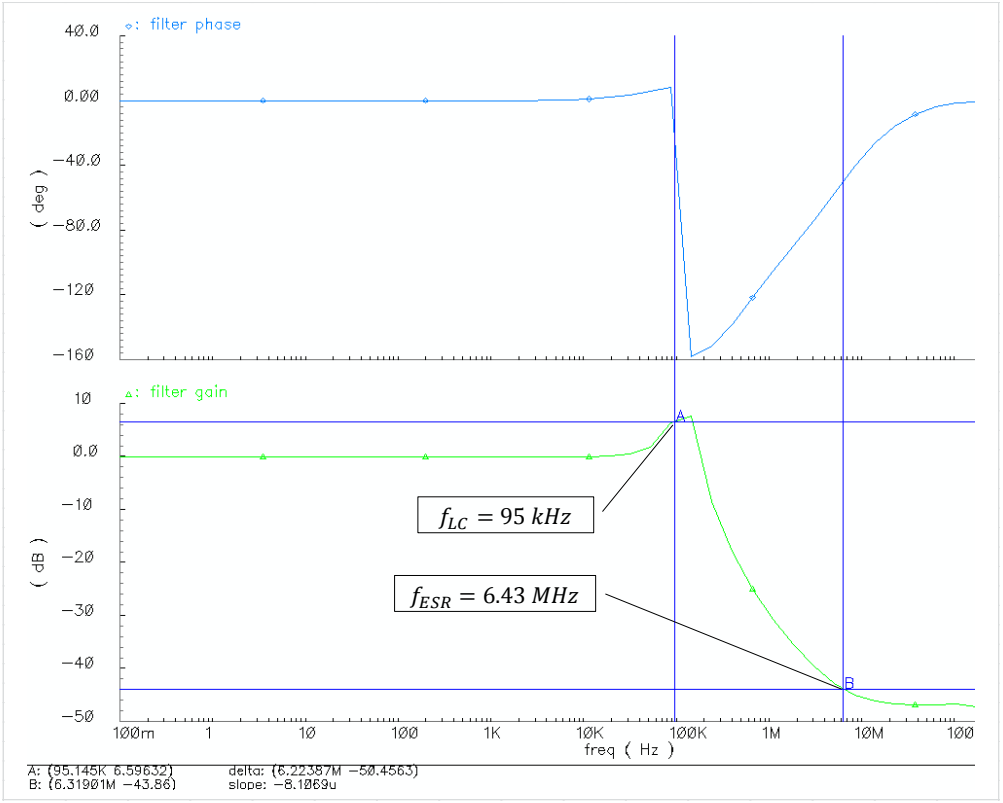

Figure 5.10 Output LC filter's Bode plot (lossy)

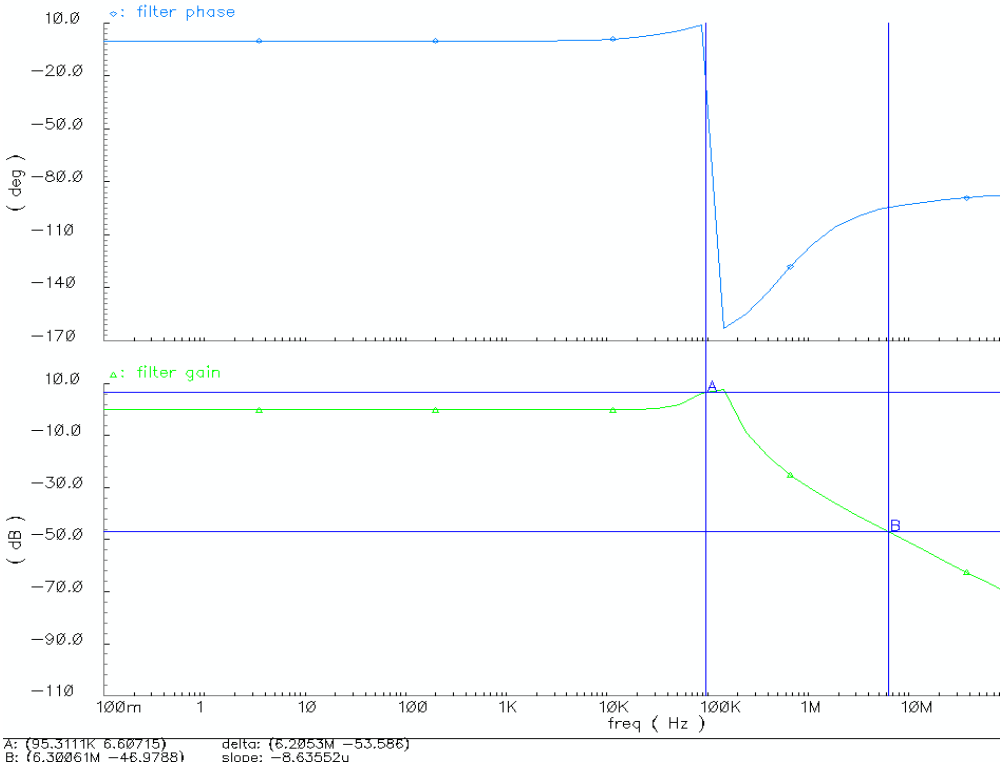

Figure 5.11 Output LC filter's Bode plot (lossless)

5.10 Output voltage and load current ripples

Figure 5.12 shows the output voltage and current ripples waveforms of DC/DC buck converter circuit under following conditions (using type III compensation network);

V_{in}= 1.1 v, V_{ref} = 500 mV, L= 8.5 µH, C_L= 330 nF, ESR= 75 mΩ, DCR= 50 mΩ, R_L= 625 Ω and switching frequency f_{sw}=20MHz. The measured ripple of output voltage and load current are 0.12 mV and 0.2µA respectively.

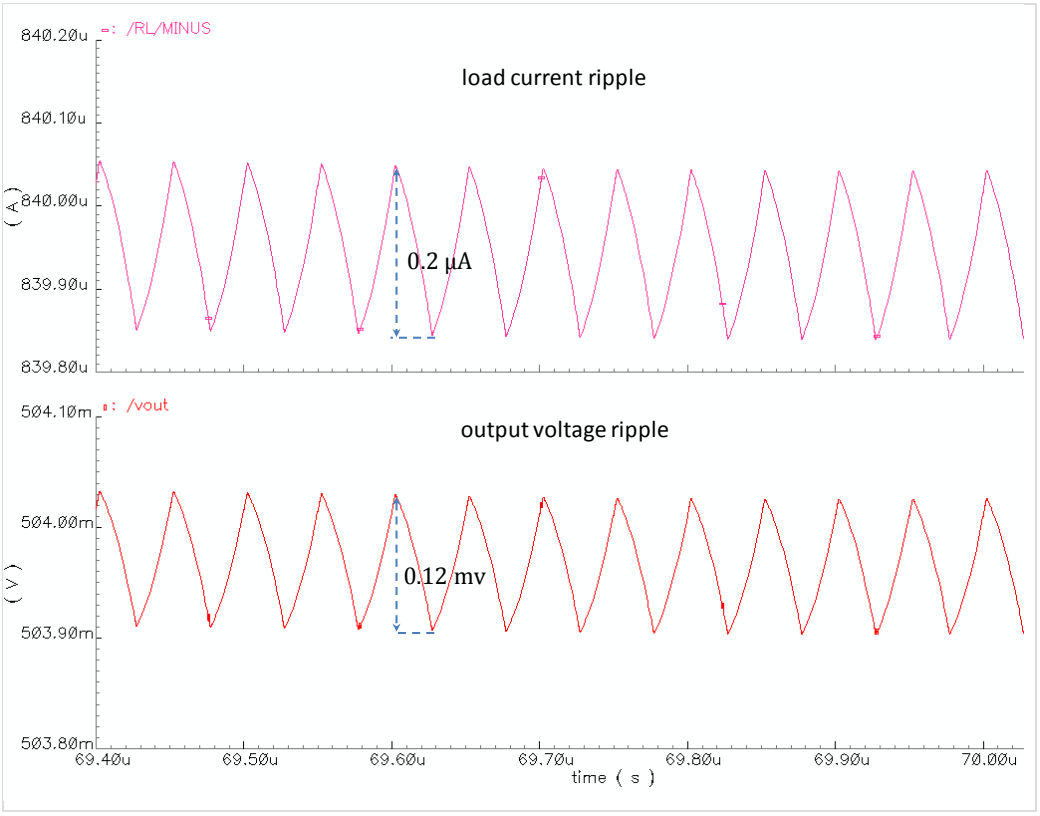

Figure 5.12 Output voltage and load current ripples using type III compensation network

As shown in figure 5.13, when type II compensation network is used instead of type III since it has not enough phase boost to assurance the system's stability the large ripples appeared at the output voltage and current load waveforms;

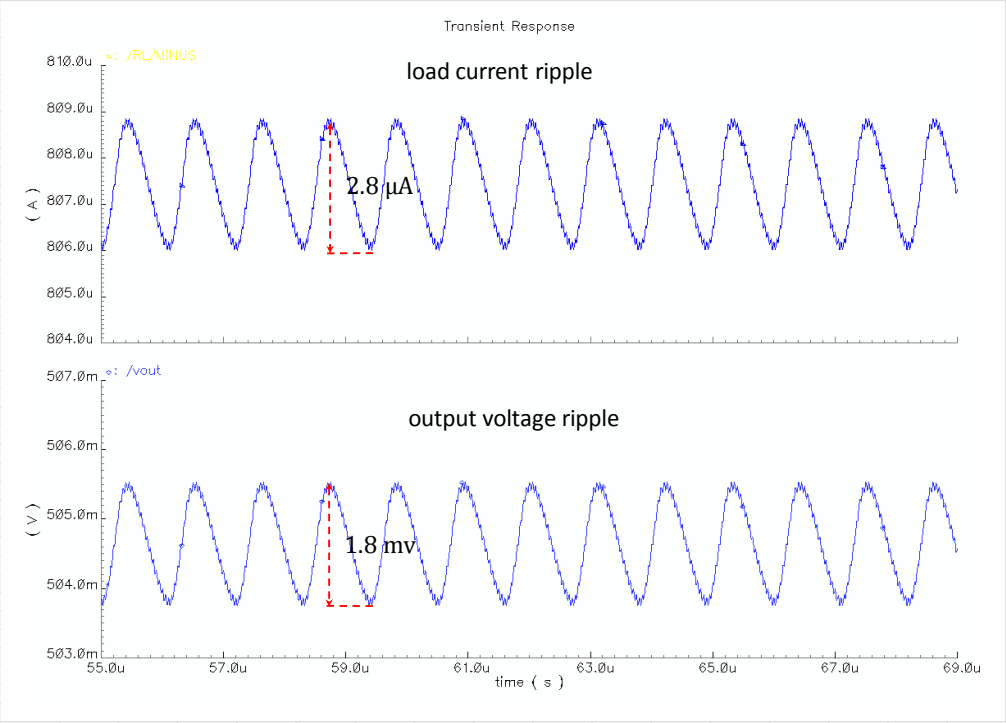

Figure 5.13 Output voltage and load current ripples using type II compensation network

5.11 Settling time

Figure 5.14 shows the time that the buck converter requires in order to regulate the output voltage based on the set reference voltage (settling time). As can be seen the settling time is around 45 µs which guarantees smooth and fast transient response of the system.

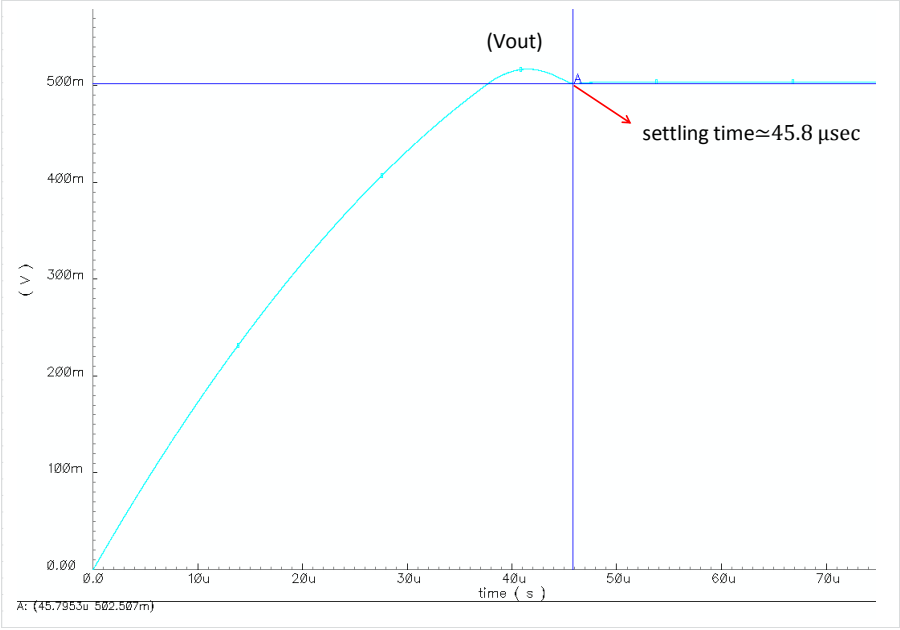

Figure 5.14 Settling time

Also figure 5.15 depicts the voltage drop across the load. As can be seen when the output voltage drops below the predefined limit set, the feedback loop forces the average inductor current to increase to regulate the output voltage V_{out} to V_{ref}. For instance when voltage drop around 200mV (due to a large change in load) occurs, approximately 25µs takes to feedback control loop can adjust the output voltage to set reference voltage (which here is 500mV).

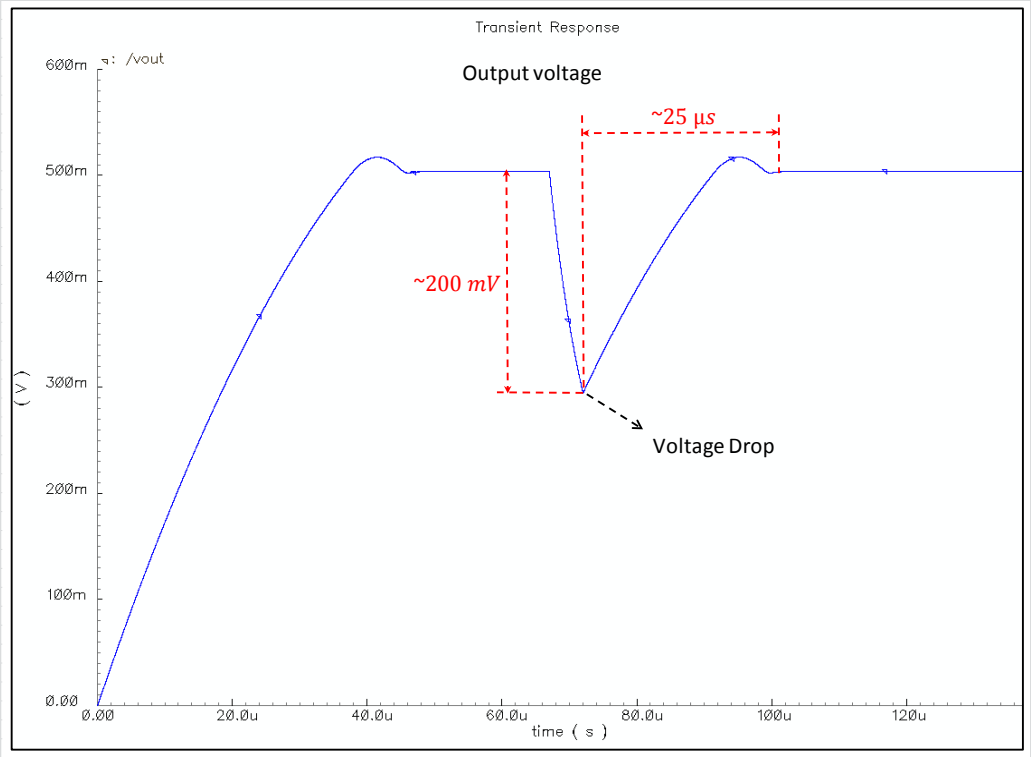

Figure 5.15 Voltage drop

5.12 Efficiency vs. load current

Figure 5.16 shows the effect of different load current on the buck converter's power efficiency η, as can be seen when the load current is in the range of "0.5 mA~1.26 mA" the converter's efficiency is over 81%.

For more discussion about the efficiency and power dissipation of DC/DC buck converter we can divide the graph 5.16 into three regions, as shown in figure 5.16. In region (I) which is related to high load, the conduction loss (due to parasitic resistive impedances) is the dominant power loss. In region II (light load) the switching loss is the major power loss in buck converter circuit. And finally in region III (very light load) the dominate power loss is the gate-drive loss caused by charging and discharging of the gate capacitances of power transistors during switching transitions [22].

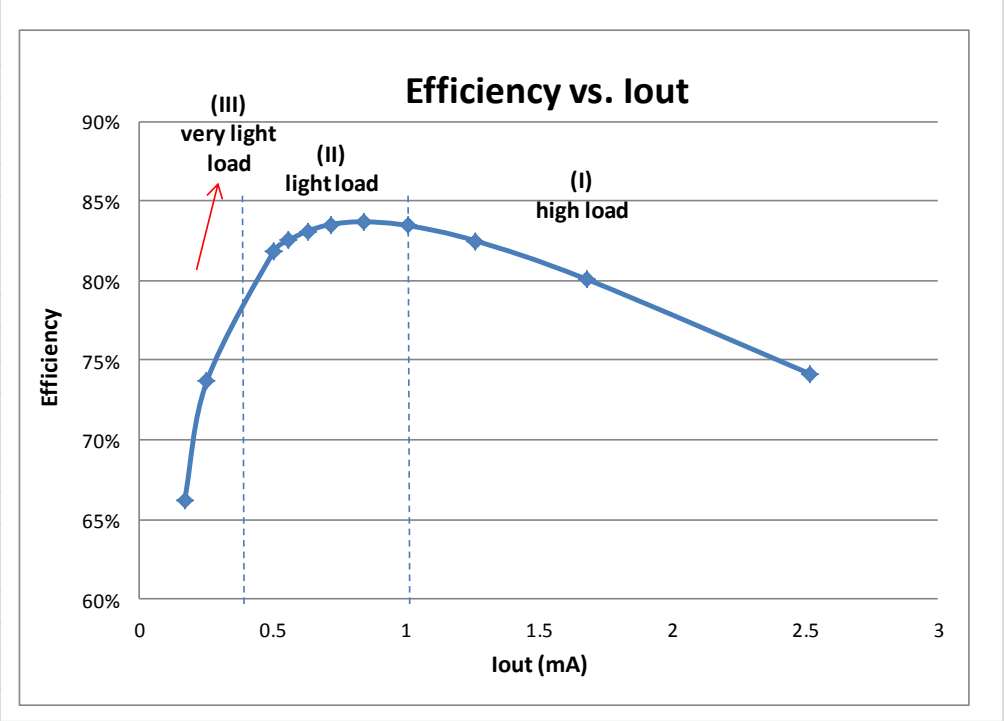

Figure 5.16 Efficiency vs. load current

Table 5.4 shows the effect of different values of load current on the output voltage and the output current ripples. As can be seen voltage and current ripple are almost the same for different values of the output current.

RL	200Ω	600Ω	1kΩ	2k Ω	3k Ω
Input Voltage	1.1v	1.1v	1.1v	1.1v	1.1v
Average Output Voltage	503.8mV	504mV	504mV	504mV	504mV
Output Current	2.519mA	840µA	504µA	252µA	168µA
Average Output power	1.269mW	423.3uW	254uW	127uW	84.67uW
Average input power	1.712mW	505.8uW	310.3uW	172.3uW	127.9uW
Switching Frequency	20MHz	20MHz	20MHz	20MHz	20MHz
Settling time	62.1µs	46.3µs	44.8µs	43.8µA	43.6µA
voltage ripple(peak to peak)	0.12mV	0.12mV	0.12mV	0.12mV	0.12mV
current ripple(peak to peak)	0.55µA	0.2µA	0.12µA	0.06µA	0.04µA
Power efficiency (%)	74.15%	83.69%	81.85%	73.7%	66.22%

Table 5.4 Effect of different values of load current on efficiency, output voltage and output current ripples

5.13 Efficiency vs. switching frequency

Figure 5.17 shows the effect of different values of switching frequency f_{sw} on the converter's power efficiency η. Resistive losses dominate at lower switching frequencies while the dominant power losses at higher switching frequencies are related to capacitive losses [23].

As can be seen the maximum efficiency is achieved when the frequency is about 40 MHz (more than 84% @ frequency 40 MHz) after this frequency the efficiency is decreased linearly due to higher capacitive losses in the output power stage.

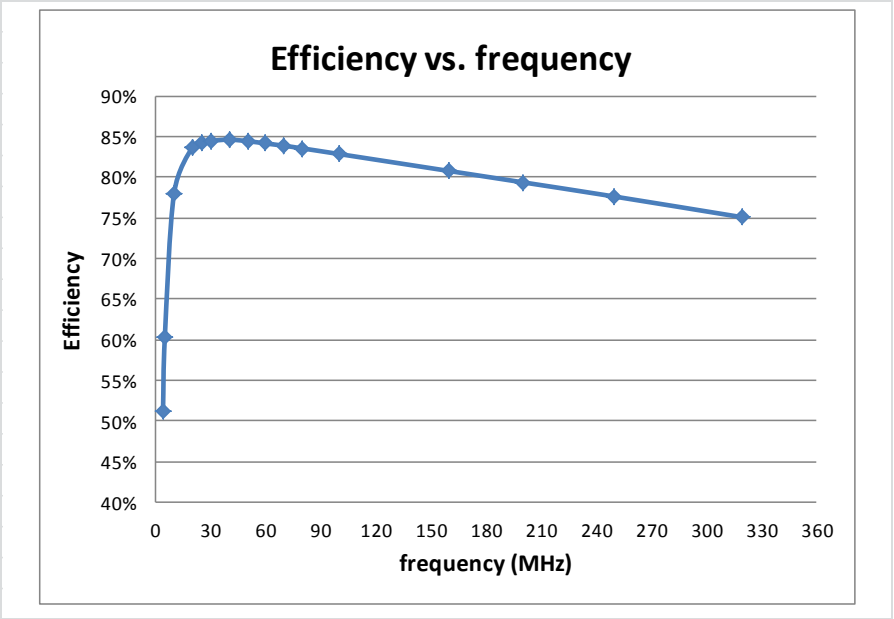

Figure 5.17 Efficiency vs. switching frequency at V_{out}=500 mV

5.14 Efficiency vs. duty cycle

Figure 5.18 shows the effect of different values of duty cycle on the buck converter's power efficiency. As can be seen efficiency of buck converter suffers from the small values of duty cycle, mostly because of increase in switching loss in the power MOSFETs [24]. The highest efficiency ($\eta = 86.6\%$) is achieved at duty cycle 0.63 where the output voltage is 700mV.

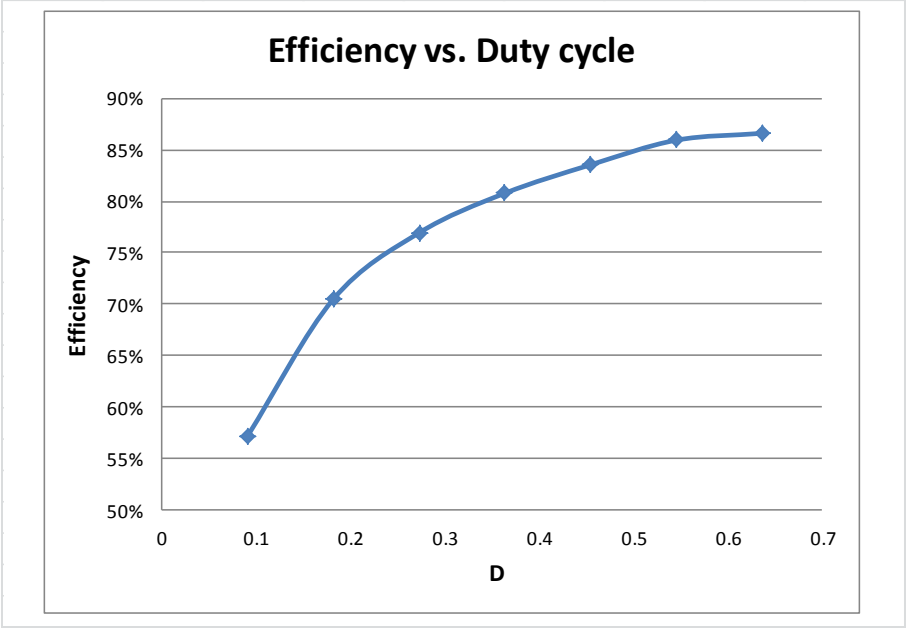

Figure 5.18 Efficiency vs. duty cycle

5.15 Performance comparison:

Compared to previously reported works, this design with such a low input and output voltage (which any voltage drops will take out a lot of efficiency) has a good power efficiency even more than 84% at frequency 40 MHz which capacitive losses are dominant at such a frequency. This accomplished by sizing the power switches to have a low parasitic output capacitance C_{DS} to avoid more power dissipation due to capacitive losses, also to overcome the gate-drive losses at very light load the gate capacitances of power MOSFETs are small enough to reduce charging and discharging time and have a faster switching time.

The voltage ripples due to switching is very low because of choosing proper components' value for compensation network and output filter, also due to wide bandwidth error amplifier the fast transient response of the system is achieved and settling time can be compared with previous works which have been done on the control loop of buck converter [27], [28], [29]. In this thesis a simplified feedback control loop is employed to reduce chip area and power dissipation in the system. Moreover the fully integrated compensation network with an accurate transient response is achieved in this work.

Chapter 6

Conclusion and future work

6.1 Conclusion

In this thesis different methods of feedback control which is used in DC/DC buck converter like voltage mode control and current mode control have been discussed. Also the structure of buck converter has been studied and its different parts are introduced. It has been shown that switching mode DC/DC converter dissipates less power than linear regulator due to using switching technique instead of variable resistance in the power stage of converter.

A schematic level of the PWM buck converter (using VMC) was implemented in 65nm CMOS technology with switching frequency 20MHz. The simulation results show that the implemented converter works efficiently when load current is in the range of 0.5 mA to 1.26 mA (power efficiency higher than 81%) and since wide bandwidth error amplifier is used in the feedback control loop of the system, it has a fast settling time (~45 μs).

The crucial part of the designing buck converter circuit is compensation network. In this thesis after a deep study about different types of compensation networks, due to low value of inductor ESR the compensation type III is employed and its elements value were calculated accurately to assurance the stability of the system and reduce the ripples at the output voltage, Also effect of changes in different factors and elements like load current, switching frequency and duty cycle on power efficiency, current and voltage ripple has been observed.

6.2 Future work

A dead-time control part can be used after comparator to avoid the short-circuit losses which occurs when the HSS (PMOS) and LSS (NMOS) conduct at the same time. Thus applying a short dead time can guarantee that both the power MOSFETs will not conduct at the same time for any period of time. Another recommendation for future work is designing the converter at the layout level in 65nm CMOS process to determine the full chip area. Also more study can be done about other modern control techniques to find a proper feedback control method which can enhance the power efficiency of this ultra-low power buck converter.

References

[1] Marian K. Kazimierczuk, *"Pulse-width Modulated DC-DC Power Converters"*, 1^{st} Edition, Wiley.

[2] Ned Mohan, Tore M. Undeland, William P. Robbins, *"Power Electronics: Converters, Applications, and Design"*, 3rd Edition, Wiley.

[3] Jerrold Foutz, *"Switching-Mode Power Supply Design Tutorial Introduction"*, SMPS Technology, http://www.smpstech.com/tutorial/t01int.htm , accessed: Mar 2012.

[4] Abraham I. Pressman, *"Switching Power Supply Design"*, Second Edition, McGraw-Hill, Publication Date: Nov 1997.

[5] Chester Simpson, "*Linear and Switching Voltage Regulator Fundamentals*", National Semiconductor, http://www.national.com/assets/en/appnotes/f4.pdf , accessed: Mar 2012.

[6] Maxim Integrated Products, Inc., "*DC-DC Converter Tutorial*", Application Note 2031, Nov 29, 2001.

[7] Ray Ridley, "*CURRENT MODE or VOLTAGE MODE ?*", Switching Power Magazine, Oct 2000, http://encon.fke.utm.my/nikd/latest/OctCurrentMode.pdf , accessed: Mar 2012.

[8] Madhuravasal Vijayaraghavan G., "*Extreme temperature switch mode power supply based on vee-square control using silicon carbide, silicon on sapphire, hybrid technology*", Doctoral Thesis, Oklahoma State University, 2009.

[9] L. K. Wong, T. K. Man, "*How to best implement a synchronous buck converter*", National Semiconductor, Apr 2008, http://www.eetimes.com/design/power-management-design/4012225/Tip-of-the-Week-How-to-best-implement-a-synchronous-buck-converter , accessed: Mar 2012.

[10] Ajith Jain, "*Synchronous vs. Aynchronous Buck Regulators*", SEMTECH Corp., http://www.digikey.com/Web%20Export/Supplier%20Content/Semtech_600/PDF/Semtech_synchronous-vs-asynchronous-buck-regulators.pdf?redirected=1 , accessed: Mar 2012.

[11] Jon Klein, "*Synchronous buck MOSFET loss calculations with Excel model*". Application note AN–6005, Fairchild Semiconductor, version 1.0.1, Apr 2006.

[12] Bill Hutchings, "*SMPS Buck Converter Design Example*", Microchip Technology Inc., http://satcom.tonnarelli.com/files/smps/SMPSBuckDesign_031809.pdf , accessed: Mar 2012.

[13] "*Buck converter*", http://en.wikipedia.org/wiki/Buck_converter , accessed: Mar 2012

[14] Daniel Meeks, "*Loop Stability Analysis of Voltage Mode Buck Regulator With Different Output Capacitor Types – Continuous and Discontinuous Modes*", Application Report SLVA301, Texas Instruments Inc., Apr 2008.

[15] A. Maity, A. Patra, N. Yamamura, J. Knight, "*Design of a 20 MHz DC-DC Buck Converter with 84% Efficiency for Portable Applications*", IEEE International Conference on VLSI Design, pp. 316 - 321, Jan 2011.

[16] Venable Instruments, "*Optimum Feedback Amplifier Design For Control Systems*", http://www.venable.biz/tp-03.pdf , accessed: Mar 2012

[17] Michael Day, "*Optimizing Low-Power DC/DC Designs – External versus Internal Compensation*", Texas Instruments Inc., http://www.ti.com/lit/ml/slyp090/slyp090.pdf , accessed: Mar 2012.

[18] Doug Mattingly, "*Designing Stable Compensation Networks for Single Phase Voltage Mode Buck Regulators*", Technical Brief TB417.1, Intersil Americas Inc., Dec 2003.

[19] N.D. Muhamad, A.J. Shafie, "*An Approach to PSpice-aided Control Loop Design of DC-DC .Converter Systems*", IEEE Power Engineering Conference (PECon) Proceedings. National, pp. 121 - 126, Dec 2003.

[20] Sipex Corp., "*Selecting Appropriate Compensation: Type-II or Type-III*", Application Note ANP18, Dec 2006, www.exar.com/Common/Content/Document.ashx?id=1241 , accessed: Mar 2012.

[21] T. Brusev, P. Goranov, M. Hristov, "*Buck converter for low power applications*", IEEE 26th International Conference on Microelectronics, pp. 447 - 450, May 2008.

[22] Siyuan Zhou, G.A. Rincon-Mora, "*A high efficiency, soft switching DC-DC converter with adaptive current-ripple control for portable applications*", IEEE Transactions on Circuits and Systems II: Express Briefs, pp. 319 - 323, Apr 2006.

[23] A. Emira, F. Carr, H. Elwan, R.H. Mekky, "*High voltage tolerant integrated Buck converter in 65nm 2.5V CMOS*", IEEE International Symposium on Circuits and Systems (ISCAS), pp. 2405 - 2408, May 2009.

[24] Peng Xu, Jia Wei, F.C. Lee, "*Multiphase coupled-buck converter-a novel high efficient 12 V voltage regulator module*", IEEE Transactions on Power Electronics, pp. 74 - 82, Jan 2003.

[25] Texas A&M University, Analog and Mixed-Signal Center, "*Low Drop-Out Voltage Regulators*", amesp02.tamu.edu/~sanchez/607%20Lect%2012%20LDO.ppt , accessed: Mar 2012.

[26] Victor Power Technologies, "*DC-to-DC Converter*", http://www.victorpower.com/knowledge_base.php , accessed: Mar 2012.

[27] O. Trescases, Z. Lukic, Wai Tung Ng, A. Prodic, "*A low-power mixed-signal current-mode DC-DC converter using a one-bit ΔΣ DAC*", Twenty-First Annual IEEE, Applied Power Electronics Conference and Exposition (APEC), pp. 700 - 704, Mar 2006.

[28] Hyun-Hee Park, Young-Jin Woo, Gyu-Hyeong Cho, "*A fully integrated wide-band PID controller with capacitor-less compensation for step-down DC-DC converter*", IEEE International Symposium on Circuits and Systems (ISCAS), pp. 506 - 509, May 2011.

[29] K. Umimura, H. Sakurai, Y. Sugimoto, "*A CMOS Current-mode DC-DC converter with input and output voltage-independent stability and frequency characteristics utilizing a quadratic slope compensation scheme*", 33rd European IEEE Solid State Circuits Conference (ESSCIRC), pp. 178 - 181, Sep 2007.

[30] Maxim Integrated Products, Inc., "An Introduction to Switch-Mode Power Supplies", Application Note 4087, Sep 27, 2007.

[31] Zhuo Bi, Wenbin Xia, "*Modeling and Simulation of Dual-Mode DC/DC Buck Converter*", Second IEEE International Conference on Computer Modeling and Simulation, (ICCMS), pp. 371 - 375, Jan 2010.

[32] Chu-Hsiang Chia, Pui-Sun Lei, Robert Chen-Hao Chang, "*A high-efficiency PWM DC-DC buck converter with a novel DCM control under light-load*", IEEE International Symposium on Circuits and Systems (ISCAS), pp. 237 - 240, May 2011.

[33] Donald Schelle, Jorge Castorena, "*Buck-Converter Design Demystified*", Power Electronics Technology, June 2006.